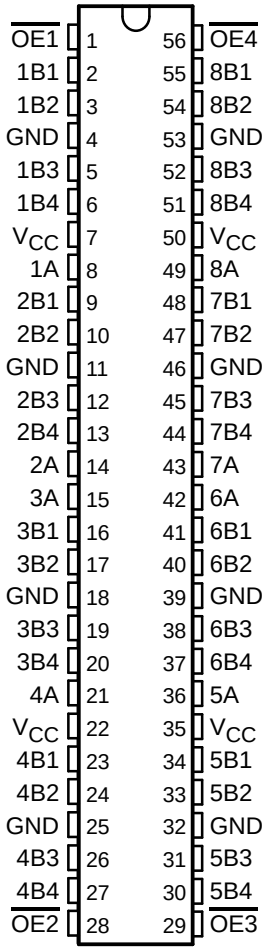
- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DGG) and Thin Shrink Small-Outline (DL) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALVCH162344 is a 1-bit-to-4-bit address driver used in applications where four separate memory locations must be addressed by a single address.

The outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH162344 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH162344 is characterized for operation from –40°C to 85°C.

A-TO-B FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Bn
L	H	H
L	L	L
H	X	Z

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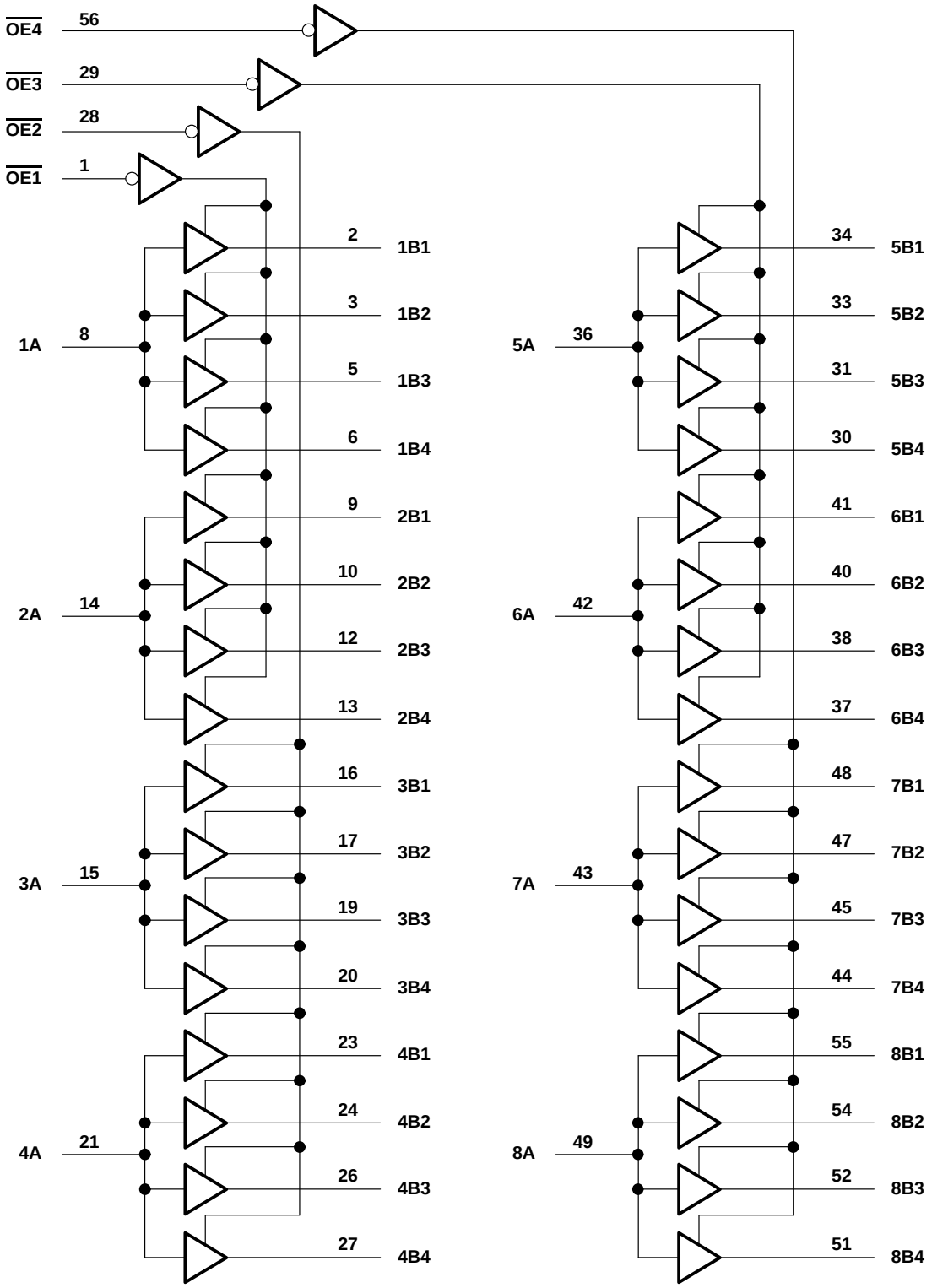
logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–6	mA
		V_{CC} = 2.7 V		–8	
		V_{CC} = 3 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –4 mA,	V_{IH} = 1.7 V	2.3 V	1.9			
		I_{OH} = –6 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –8 mA,	V_{IH} = 2 V	2.7 V	2			
		I_{OH} = –12 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 4 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 6 mA	V_{IL} = 0.7 V	2.3 V			0.55	
			V_{IL} = 0.8 V	3 V			0.55	
		I_{OL} = 8 mA,	V_{IL} = 0.8 V	2.7 V			0.6	
		I_{OL} = 12 mA,	V_{IL} = 0.8 V	3 V			0.8	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V				pF
	Data inputs							
C_o	Outputs	V_O= V_{CC} or GND		3.3 V				pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B							ns
t_{en}	$\overline{OE}$	B							ns
t_{dis}	$\overline{OE}$	B							ns
$t_{sk(o)}$§									ns
$t_{sk(o)}$¶									ns

§ Skew between outputs of the same bank and same package (same transition). This parameter is warranted but not production tested.
¶ Skew between outputs of all banks of same package (A1–A8 tied together). This parameter is warranted but not production tested.

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 0, f = 10 MHz			pF
		Outputs disabled				

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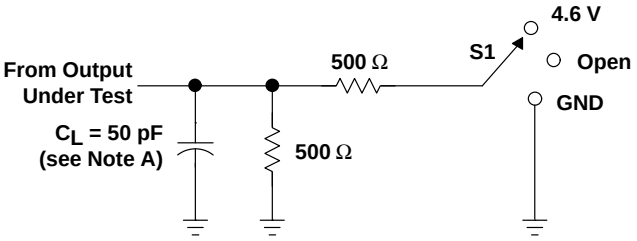
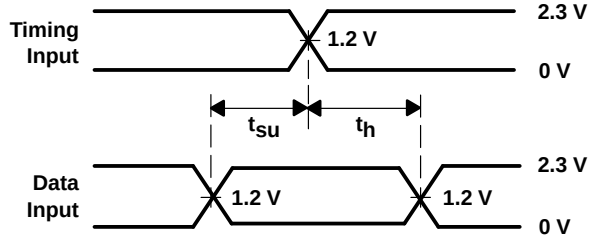
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

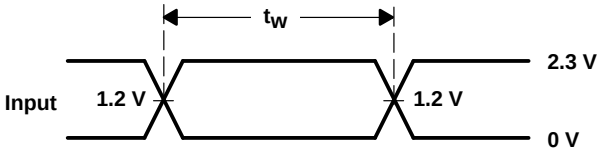


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

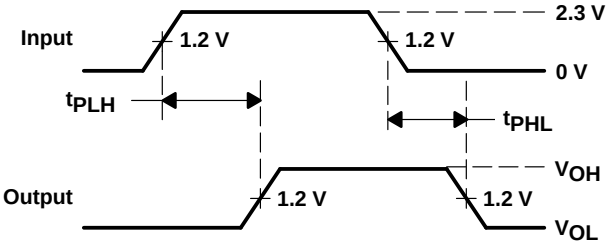
LOAD CIRCUIT



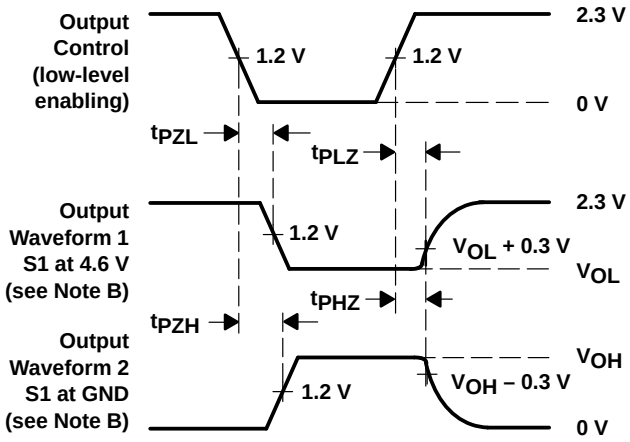
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



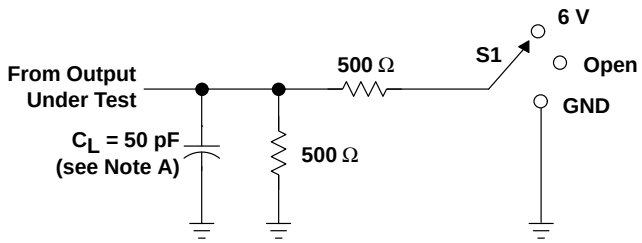
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

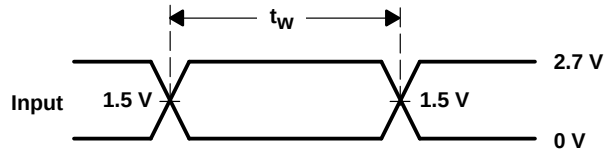
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

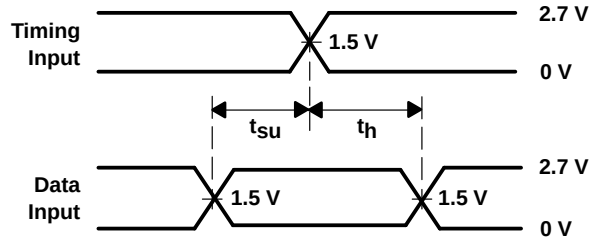


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

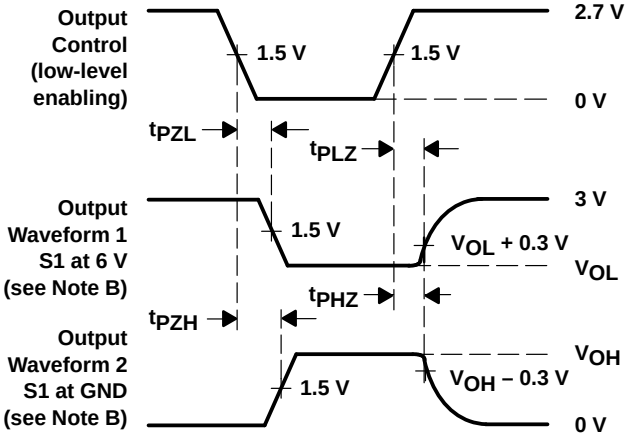
LOAD CIRCUIT



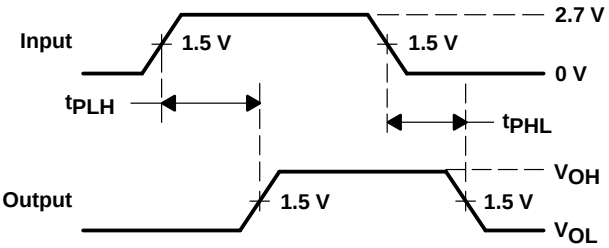
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

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D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

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