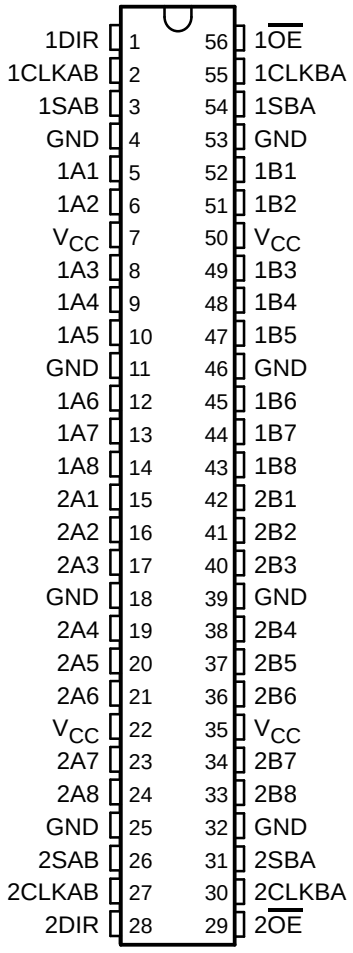
- **Members of the Texas Instruments *Widebus*™ Family**
- **High-Impedance State During Power Up and Power Down**
- **5-V I/O Compatible**
- **High-Drive Outputs (–32 mA/64 mA)**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Auto 3-State Eliminates Bus Current Loading When Voltage at the Output Exceeds $V_{CC}$**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup/Pulldown Resistors**
- **Power Off Disables Inputs/Outputs, Permitting Live Insertion**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package**

**SN54ALVTH16646 . . . WD PACKAGE**
**SN74ALVTH16646 . . . DGG, DGV, OR DL PACKAGE**
**(TOP VIEW)**




PRODUCT PREVIEW

## description

The ’ALVTH16646 are 16-bit bus transceivers designed for 2.5-V or 3.3-V $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ′ALVTH16646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

## description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When $V_{CC}$ is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVTH16646 is available in TI's thin very small-outline package (DGV), which provides the same I/O pin count and functionality of standard Widebus packages in less than half the printed circuit board area.

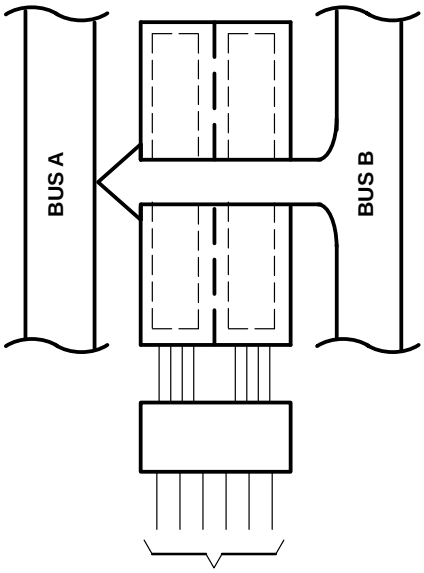
The SN54ALVTH16646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALVTH16646 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | | | | DATA I/OS | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA | A1 – A8 | B1 – B8 | |
| X | X | = | X | X | X | Input | Unspecified† | Store A, B unspecified† |
| X | X | X | ↑ | X | X | Unspecified† | Input | Store B, A unspecified† |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| H | X | H or L | H or L | X | X | Input disabled | Input disabled | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| L | H | H or L | X | H | X | Input | Output | Stored A data to B bus |

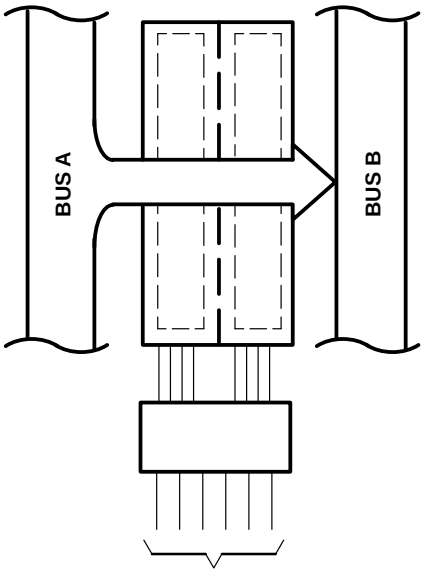
† The data output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

PRODUCT PREVIEW



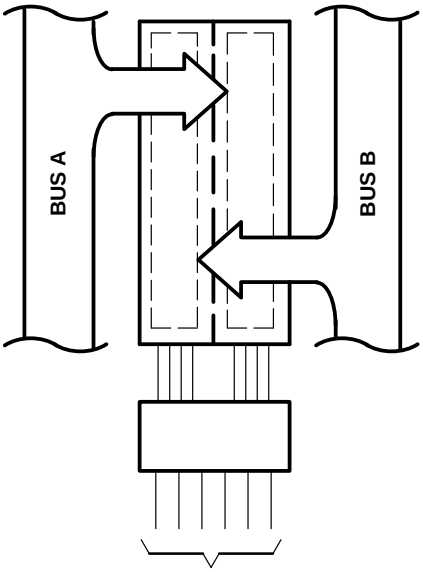

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**



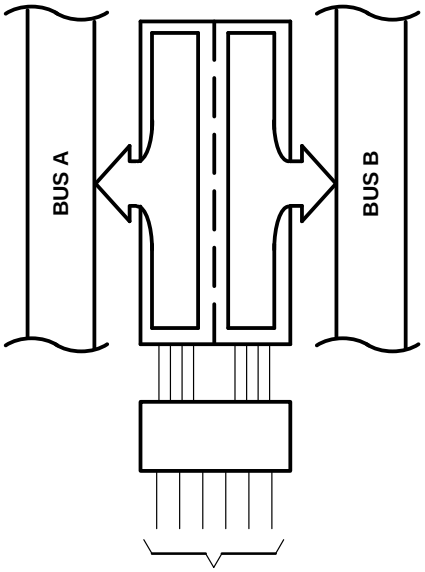

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | H | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**




| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| X | X | ↑ | X | X | X |
| X | X | X | ↑ | X | X |
| H | X | ↑ | ↑ | X | X |

**STORAGE FROM**
**A, B, OR A AND B**



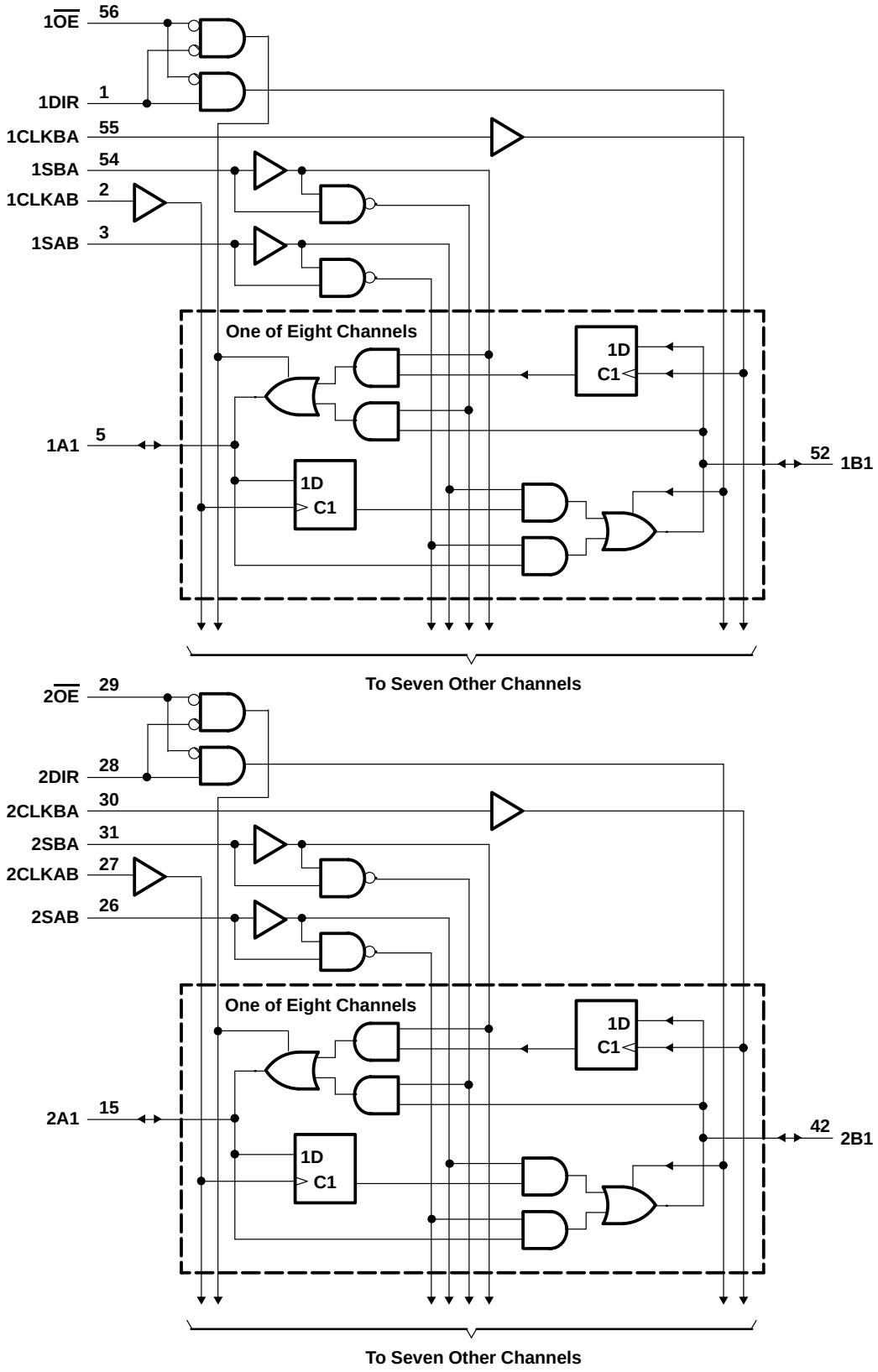

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | H or L | X | H |
| L | H | H or L | X | H | X |

**TRANSFER STORED DATA**
**TO A AND/OR B**

**Figure 1. Bus-Management Functions**

PRODUCT PREVIEW

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) . . . . –0.5 V to 7 V
Output current in the low state, $I_O$: SN54ALVTH16646 . . . . . 96 mA
SN74ALVTH16646 . . . . . 128 mA
Output current in the high state, $I_O$: SN54ALVTH16646 . . . . . –48 mA
SN74ALVTH16646 . . . . . –64 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DGG package . . . . . 1 W
DGV package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

### recommended operating conditions, $V_{CC}$ = 2.5 V ± 0.2 V (see Note 3)

| | | | SN54ALVTH16646 | | SN74ALVTH16646 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.3 | 2.7 | 2.3 | 2.7 | V |
| $V_{IH}$ | High-level input voltage | | 1.7 | | 1.7 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.7 | | 0.7 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –6 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | | 6 | | 8 | mA |
| | Low-level output current; current duty cycle ≤ 50%; f ≥ 1 KHz | | | 18 | | 24 | |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

### recommended operating conditions, $V_{CC}$ = 3.3 V ± 0.3 V (see Note 3)

| | | | SN54ALVTH16646 | | SN74ALVTH16646 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 3 | 3.6 | 3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | 32 | mA |
| | Low-level output current; current duty cycle ≤ 50%; f ≥ 1 KHz | | | 48 | | 64 | |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

**electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 2)**

| PARAMETER | TEST CONDITIONS | | | SN54ALVTH16646 | | | SN74ALVTH16646 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 2.3 V, | $I_I$ = –18 mA | | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 2.3 V to 2.7 V, | $I_{OH}$ = –100 µA | | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | $V_{CC}$ = 2.3 V | $I_{OH}$ = – 6 mA | | 1.7 | | | | | | |
| | | $I_{OH}$ = – 8 mA | | | | | 1.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 2.3 V to 2.7 V, | $I_{OL}$ = 100 µA | | | | 0.2 | | | 0.2 | V |
| | $V_{CC}$ = 2.3 V | $I_{OL}$ = 6 mA | | | | 0.5 | | | | |
| | | $I_{OL}$ = 8 mA | | | | | | | 0.5 | |
| | | $I_{OL}$ = 18 mA | | | | 0.5 | | | | |
| | | $I_{OL}$ = 24 mA | | | | | | | 0.5 | |
| $I_I$ | $V_{CC}$ = 2.7 V, | $V_I$ = GND | Control inputs | | | ±1 | | | ±1 | µA |
| | $V_{CC}$ = 0 or 2.7 V, | $V_I$ = 2.7 V | | | | 10 | | | 10 | |
| | $V_{CC}$ = 2.7 V | $V_I$ = $V_{CC}$ | A or B ports | | | 10 | | | 10 | |
| | | $V_I$ = 0 | | | | –5 | | | –5 | |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | ±100 | | | ±100 | µA |
| $I_{I(hold)}$ | $V_{CC}$ = 2.3 V | $V_I$ = 0.7 V | A or B ports | | 90 | | | 90 | | µA |
| | | $V_I$ = 1.7 V | | | 75 | | | 75 | | |
| | $V_{CC}$ = 2.7 V‡, | $V_I$ = 0 to 2.7 V | | | | | | | | |
| $I_{EX}$§ | $V_{CC}$ = 2.3 V, | $V_O$ = 3.6 V | | | | | | | | µA |
| $I_{OZ(PU/PD)}$¶ | $V_{CC}$ ≤ 1.2 V, $V_I$ = GND or $V_{CC}$, | $V_O$ = 0.5 V to $V_{CC}$, $\overline{OE}$ = don't care | | | | ±100 | | | ±100 | µA |
| $I_{CC}$ | $V_{CC}$ = 2.7 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | Outputs high | | 0.04 | 0.09 | | 0.04 | 0.09 | mA |
| | | | Outputs low | | 2.3 | 4.5 | | 2.3 | 4.5 | |
| | | | Outputs disabled | | 0.04 | 0.09 | | 0.04 | 0.09 | |
| $C_i$ | $V_{CC}$ = 2.5 V, | $V_I$ = 2.5 V or 0 | | | 3 | | | 3 | | pF |
| $C_{io}$ | $V_{CC}$ = 2.5 V, | $V_O$ = 2.5 V or 0 | | | 9 | | | 9 | | pF |

† All typical values are at $V_{CC}$ = 2.5 V, $T_A$ = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ Current into an output in the high state when $V_O$ > $V_{CC}$
¶ High-impedance state during power up/high-impedance state during power down

**electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)**

| PARAMETER | TEST CONDITIONS | | | SN54ALVTH16646 | | | SN74ALVTH16646 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 3 V, | $I_I$ = –18 mA | | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 3 V to 3.6 V, | $I_{OH}$ = –100 µA | | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | $V_{CC}$ = 3 V | $I_{OH}$ = – 24 mA | | 2 | | | | | | |
| | | $I_{OH}$ = – 32 mA | | | | | 2 | | | |
| $V_{OL}$ | $V_{CC}$ = 3 V to 3.6 V, | $I_{OL}$ = 100 µA | | | | 0.2 | | | 0.2 | V |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | | | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | | | | 0.5 | | | | |
| | | $I_{OL}$ = 32 mA | | | | | | | 0.5 | |
| | | $I_{OL}$ = 48 mA | | | | 0.55 | | | | |
| | | $I_{OL}$ = 64 mA | | | | | | | 0.55 | |
| $I_I$ | $V_{CC}$ = 3.6 V, | $V_I$ = VCC or GND | Control inputs | | | ±1 | | | ±1 | µA |
| | $V_{CC}$ = 0 or 3.6 V, | $V_I$ = 5.5 V | Control inputs | | | 10 | | | 10 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | A or B ports | | | 20 | | | 20 | |
| | | $V_I$ = $V_{CC}$ | A or B ports | | | 10 | | | 10 | |
| | | $V_I$ = 0 | A or B ports | | | –5 | | | –5 | |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | ±100 | | | ±100 | µA |
| $I_{I(hold)}$ | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | A or B ports | 75 | | | 75 | | | µA |
| | | $V_I$ = 2 V | A or B ports | –75 | | | –75 | | | |
| | $V_{CC}$ = 3.6 V‡, | $V_I$ = 0 to 3.6 V | A or B ports | | | ±500 | | | ±500 | |
| $I_{EX}$§ | $V_{CC}$ = 3 V, | $V_O$ = 5.5 V | | | | 125 | | | 125 | µA |
| $I_{OZ(PU/PD)}$¶ | $V_{CC}$ ≤ 1.2 V, $V_I$ = GND or $V_{CC}$, | $V_O$ = 0.5 V to $V_{CC}$, $\overline{OE}$ = don't care | | | | ±100 | | | ±100 | µA |
| $I_{CC}$ | $V_{CC}$ = 3.6 V, $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0, | Outputs high | | 0.07 | 0.09 | | 0.07 | 0.09 | mA |
| | | | Outputs low | | 3.2 | 5 | | 3.2 | 5 | |
| | | | Outputs disabled | | 0.07 | 0.09 | | 0.07 | 0.09 | |
| $\Delta I_{CC}$# | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ –0.6 V, Other inputs at $V_{CC}$ or GND | | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | $V_{CC}$ = 3.3 V, | $V_I$ = 3.3 V or 0 | | | 3 | | | 3 | | pF |
| $C_{io}$ | $V_{CC}$ = 3.3 V, | $V_O$ = 3.3 V or 0 | | | 9 | | | 9 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ Current into an output in the high state when $V_O$ > $V_{CC}$
¶ High-impedance state during power up/high-impedance state during power down
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

PRODUCT PREVIEW

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 2)**

| | | | SN54ALVTH16646 | | SN74ALVTH16646 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 150 | 0 | 150 | MHz |
| $t_w$ | Pulse duration, CLK high or low | | 1.5 | | 1.5 | | ns |
| $t_{su}$ | Setup time, A or B before CLKAB↑ or CLKBA↑ | Data high | 2.5 | | 2.5 | | ns |
| | | Data low | 2.6 | | 2.6 | | |
| $t_h$ | Hold time, A or B after CLKAB↑ or CLKBA↑ | Data high | 0 | | 0 | | ns |
| | | Data low | 0 | | 0 | | |

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)**

| | | | SN54ALVTH16646 | | SN74ALVTH16646 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 150 | 0 | 150 | MHz |
| $t_w$ | Pulse duration, CLK high or low | | 1.5 | | 1.5 | | ns |
| $t_{su}$ | Setup time, A or B before CLKAB↑ or CLKBA↑ | Data high | 2.1 | | 2.1 | | ns |
| | | Data low | 2.2 | | 2.2 | | |
| $t_h$ | Hold time, A or B after CLKAB↑ or CLKBA↑ | Data high | 0 | | 0 | | ns |
| | | Data low | 0 | | 0 | | |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 2)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ALVTH16646 | | SN74ALVTH16646 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | TYP† | MAX | |
| $f_{max}$ | | | 150 | | 150 | | | MHz |
| $t_{pd}$ | A or B | B or A | 1.2 | 4.5 | 1.2 | 2.3 | 4.1 | ns |
| | CLKBA or CLKAB | A or B | 1.5 | 6.1 | 1.5 | 3 | 5.5 | |
| | SBA or SAB‡ | A or B | 1.5 | 6.6 | 1.5 | 3.4 | 6 | |
| $t_{en}$ | $\overline{OE}$ | A or B | 2 | 7.1 | 2 | 3.4 | 6.4 | ns |
| $t_{dis}$ | $\overline{OE}$ | A or B | 2 | 7.8 | 2 | 4.2 | 7.1 | ns |
| $t_{en}$ | DIR | A or B | 2 | 7.2 | 2 | 3.5 | 6.5 | ns |
| $t_{dis}$ | DIR | A or B | 2 | 7.9 | 2 | 4.3 | 7.1 | ns |

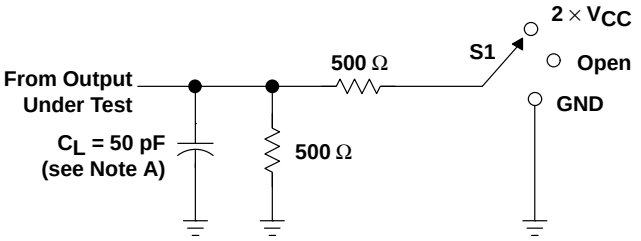
† All typical values are at $V_{CC}$ = 2.5 V, $T_A$ = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

**switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ALVTH16646 | | SN74ALVTH16646 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | TYP§ | MAX | |
| $f_{max}$ | | | 150 | | 150 | | | MHz |
| $t_{pd}$ | A or B | B or A | 1 | 3.1 | 1 | 1.8 | 2.8 | ns |
| | CLKBA or CLKAB | A or B | | 3.8 | | 2.4 | 3.4 | |
| | SBA or SAB‡ | A or B | 1.4 | 4.4 | 1.4 | 2.4 | 4 | |
| $t_{en}$ | $\overline{OE}$ | A or B | 1 | 4.9 | 1 | 2.6 | 4.4 | ns |
| $t_{dis}$ | $\overline{OE}$ | A or B | 1.5 | 6 | 1.5 | 3.4 | 5.4 | ns |
| $t_{en}$ | DIR | A or B | 1 | 5 | 1 | 2.6 | 4.5 | ns |
| $t_{dis}$ | DIR | A or B | 1.5 | 6 | 1.5 | 3.5 | 5.4 | ns |

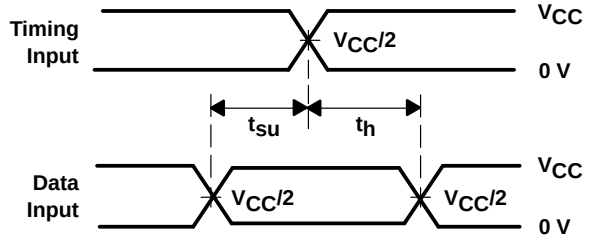
§ All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

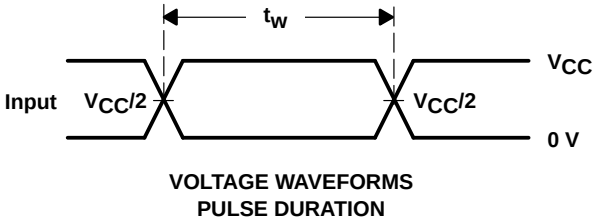



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

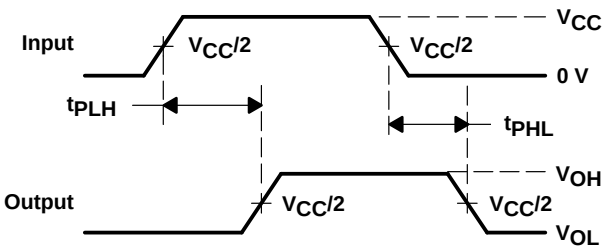
LOAD CIRCUIT



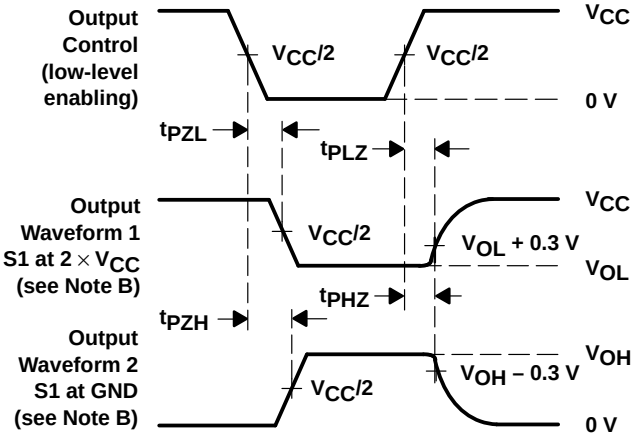

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

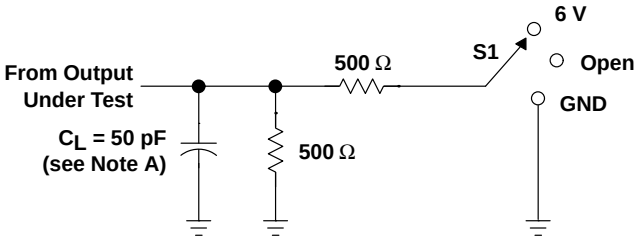



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

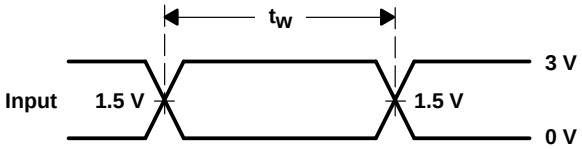
**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 3.3 V ± 0.3 V

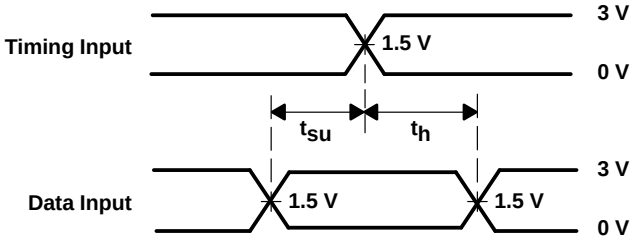



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

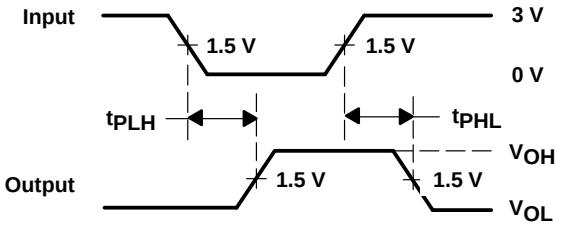
LOAD CIRCUIT



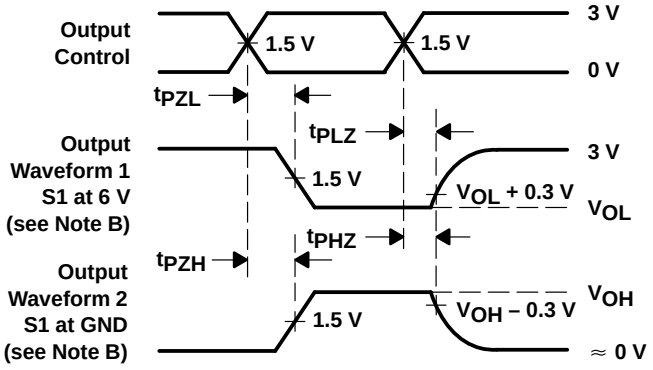

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 3. Load Circuit and Voltage Waveforms**

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