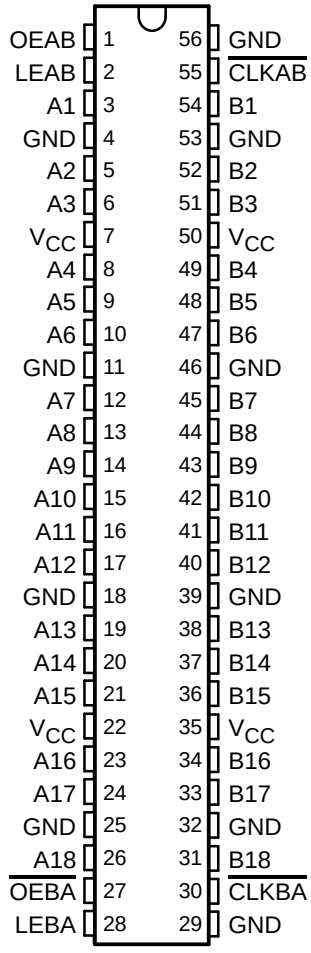
- **Members of the Texas Instruments *Widebus*™ Family**
- **High-Impedance State During Power Up and Power Down**
- **5-V I/O Compatible**
- **High-Drive Outputs (–32 mA/64 mA)**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Auto 3-State Eliminates Bus Current Loading When Voltage at the Output Exceeds V_{CC}**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup/Pulldown Resistors**
- **Power Off Disables Inputs/Outputs, Permitting Live Insertion**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package**

SN54ALVTH16500 . . . WD PACKAGE
SN74ALVTH16500 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The ’ALVTH16500 are 18-bit universal bus transceivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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description (continued)

The SN74ALVTH16500 is available in TI's thin very small-outline package (DGV), which provides the same I/O pin count and functionality of standard Widebus packages in less than half the printed circuit board area.

The SN54ALVTH16500 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALVTH16500 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	$\overline{\text{CLKAB}}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

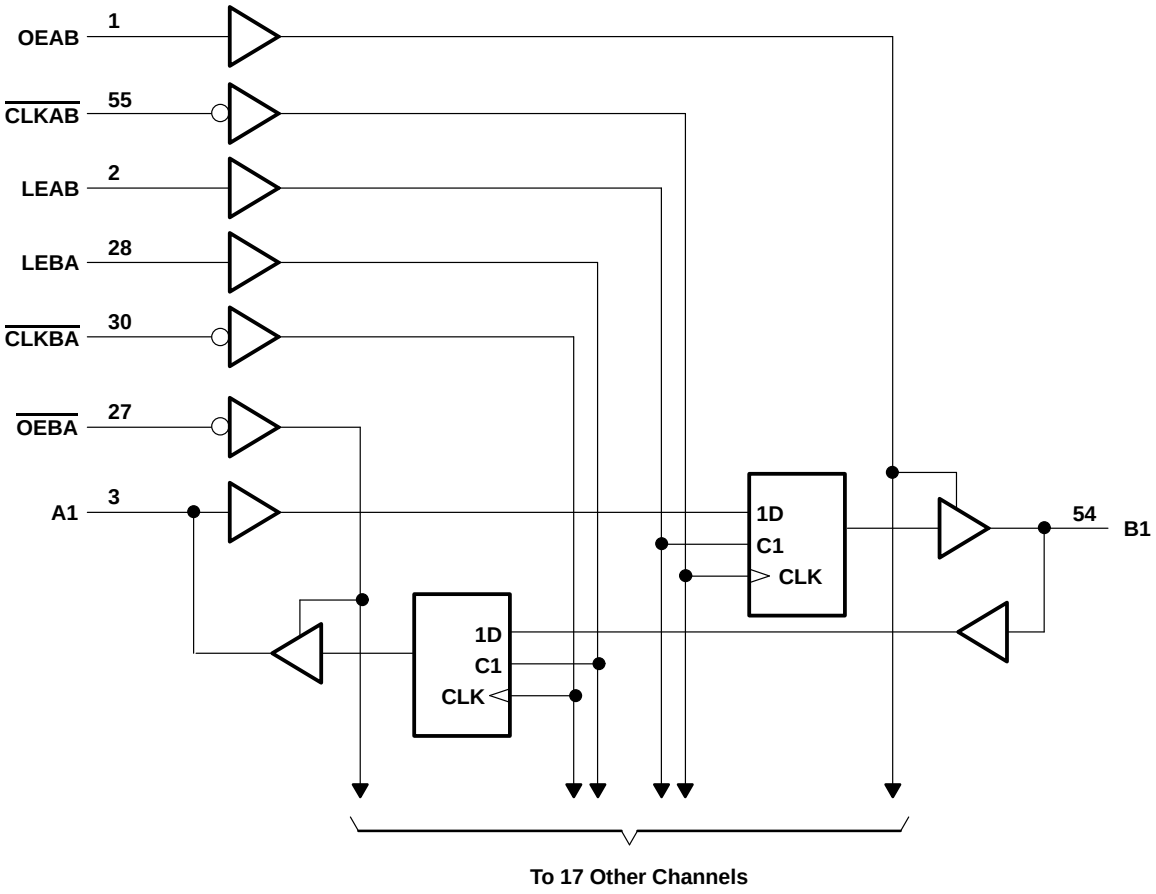
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.

‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) . . . . –0.5 V to 7 V
Output current in the low state, I_O: SN54ALVTH16500 . . . . . 96 mA
SN74ALVTH16500 . . . . . 128 mA
Output current in the high state, I_O: SN54ALVTH16500 . . . . . –48 mA
SN74ALVTH16500 . . . . . –64 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package . . . . . 1 W
DGV package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

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recommended operating conditions, V_{CC} = 2.5 V ± 0.2 V (see Note 3)

			SN54ALVTH16500		SN74ALVTH16500		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.3	2.7	2.3	2.7	V
V_{IH}	High-level input voltage		1.7		1.7		V
V_{IL}	Low-level input voltage			0.7		0.7	V
V_I	Input voltage		0	5.5	0	5.5	V
I_{OH}	High-level output current			–6		–8	mA
I_{OL}	Low-level output current			6		8	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 KHz			18		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

recommended operating conditions, V_{CC} = 3.3 V ± 0.3 V (see Note 3)

			SN54ALVTH16500		SN74ALVTH16500		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		3	3.6	3	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	5.5	0	5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			24		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 KHz			48		64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS			SN54ALVTH16500			SN74ALVTH16500			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.3 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = 2.3 V to 2.7 V,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.3 V	I_{OH} = – 6 mA		1.7						
		I_{OH} = – 8 mA					1.7			
V_{OL}	V_{CC} = 2.3 V to 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.3 V	I_{OL} = 6 mA				0.5				
		I_{OL} = 8 mA							0.5	
		I_{OL} = 18 mA				0.5				
		I_{OL} = 24 mA							0.5	
I_I	V_{CC} = 2.7 V,	V_I = GND	Control inputs			±1			±1	µA
	V_{CC} = 0 or 2.7 V,	V_I = 2.7 V				10			10	
	V_{CC} = 2.7 V	V_I = V_{CC}	A or B ports			10			10	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V				±100			±100	µA
$I_{I(hold)}$	V_{CC} = 2.3 V	V_I = 0.7 V	A or B ports		90			90		µA
		V_I = 1.7 V			75			75		
	V_{CC} = 2.7 V‡,	V_I = 0 to 2.7 V								
I_{EX}§	V_{CC} = 2.3 V,	V_O = 3.6 V								µA
$I_{OZ(PU/PD)}$¶	V_{CC} ≤ 1.2 V, V_I = GND or V_{CC},	V_O = 0.5 V to V_{CC}, $\overline{OE}$/OE = don't care				±100			±100	µA
I_{CC}	V_{CC} = 2.7 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		0.04	0.09		0.04	0.09	mA
			Outputs low		2.3	4.5		2.3	4.5	
			Outputs disabled		0.04	0.09		0.04	0.09	
C_i	V_{CC} = 2.5 V,	V_I = 2.5 V or 0			3			3		pF
C_{io}	V_{CC} = 2.5 V,	V_O = 2.5 V or 0			9			9		pF

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ Current into an output in the high state when V_O > V_{CC}
¶ High-impedance state during power up/high-impedance state during power down

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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	TEST CONDITIONS			SN54ALVTH16500			SN74ALVTH16500			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = 3 V to 3.6 V,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = – 32 mA					2			
V_{OL}	V_{CC} = 3 V to 3.6 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 3 V	I_{OL} = 16 mA							0.4	
		I_{OL} = 24 mA				0.5				
		I_{OL} = 32 mA							0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = VCC or GND	Control inputs			±1			±1	µA
	V_{CC} = 0 or 3.6 V,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports			20			20	
		V_I = V_{CC}				10			10	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V				±100			±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
	V_{CC} = 3.6 V‡,	V_I = 0 to 3.6 V				±500			±500	
I_{EX}§	V_{CC} = 3 V,	V_O = 5.5 V				125			125	µA
$I_{OZ(PU/PD)}$¶	V_{CC} ≤ 1.2 V, V_I = GND or V_{CC},	V_O = 0.5 V to V_{CC}, $\overline{OE}$/OE = don't care				±100			±100	µA
I_{CC}	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		0.07	0.09		0.07	0.09	mA
			Outputs low		3.2	5		3.2	5	
			Outputs disabled		0.07	0.09		0.07	0.09	
ΔI_{CC}#	V_{CC} = 3 V to 3.6 V, One input at V_{CC} –0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	V_{CC} = 3.3 V,	V_I = 3.3 V or 0			3			3		pF
C_{io}	V_{CC} = 3.3 V,	V_O = 3.3 V or 0			9			9		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ Current into an output in the high state when V_O > V_{CC}
¶ High-impedance state during power up/high-impedance state during power down
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			SN54ALVTH16500		SN74ALVTH16500		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	MHz
t_w	Pulse duration	LE high	1.5		1.5		ns
		$\overline{CLK}$ high or low	1.5		1.5		
t_{su}	Setup time	A or B before $\overline{CLKAB}$↓, Data high	2.3		2.3		ns
		A or B before $\overline{CLKBA}$↓, Data low	3.4		3.4		
		A or B before LE↓, $\overline{CLK}$ high	–0.4		–0.4		
		A or B before LE↓, $\overline{CLK}$ low	0.9		0.9		
t_h	Hold time	A or B after $\overline{CLK}$↓, Data high	0		0		ns
		A or B after $\overline{CLK}$↓, Data low	–0.7		–0.7		
		A or B after LE↓, $\overline{CLK}$ high	2		2		
		A or B after LE↓, $\overline{CLK}$ low	0.3		0.3		

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

			SN54ALVTH16500		SN74ALVTH16500		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	MHz
t_w	Pulse duration	LE high	1.5		1.5		ns
		$\overline{CLK}$ high or low	1.5		1.5		
t_{su}	Setup time	A or B before $\overline{CLKAB}$↓, Data high	1.9		1.9		ns
		A or B before $\overline{CLKBA}$↓, Data low	2.5		2.5		
		A or B before LE↓, $\overline{CLK}$ high	0		0		
		A or B before LE↓, $\overline{CLK}$ low	0.3		0.3		
t_h	Hold time	A or B after $\overline{CLK}$↓, Data high	0		0		ns
		A or B after $\overline{CLK}$↓, Data low	0		0		
		A or B after LE↓, $\overline{CLK}$ high	1.8		1.8		
		A or B after LE↓, $\overline{CLK}$ low	1.2		1.2		

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16500		SN74ALVTH16500			UNIT
			MIN	MAX	MIN	TYP†	MAX	
f_{max}			150		150			MHz
t_{pd}	B or A	A or B	1	5	1	2.5	4.5	ns
	LEBA or LEAB	A or B	2	7.2	2	3.8	6.5	
	$\overline{\text{CLKBA}}$ or $\overline{\text{CLKAB}}$	A or B	2	7.7	2	3.2	7	
t_{en}	$\overline{\text{OEBA}}$ or OEAB	A or B	2.5	7.7	2.5	4.8	6.9	ns
t_{dis}	$\overline{\text{OEBA}}$ or OEAB	A or B	3	7.7	3	4.1	6.9	ns

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16500		SN74ALVTH16500			UNIT
			MIN	MAX	MIN	TYP‡	MAX	
f_{max}			150		150			MHz
t_{pd}	B or A	A or B	1	3.4	1	2	3.1	ns
	LEBA or LEAB	A or B	1.5	6	1.5	3.2	5.4	
	$\overline{\text{CLKBA}}$ or $\overline{\text{CLKAB}}$	A or B	1.5	4.8	1.5	2.6	4.3	
t_{en}	$\overline{\text{OEBA}}$ or OEAB	A or B	1.5	6.2	1.5	3.5	5.6	ns
t_{dis}	$\overline{\text{OEBA}}$ or OEAB	A or B	2	5.5	2	3.2	4.9	ns

‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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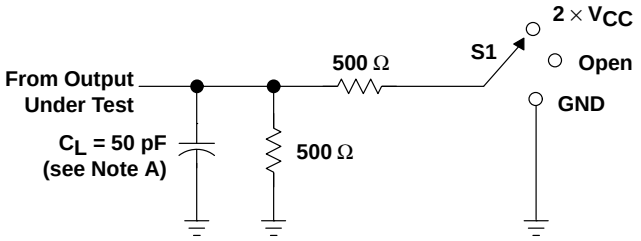
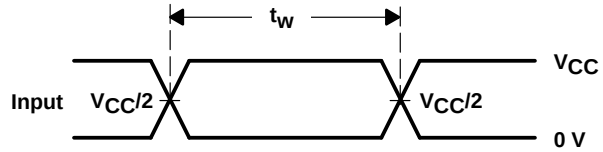
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

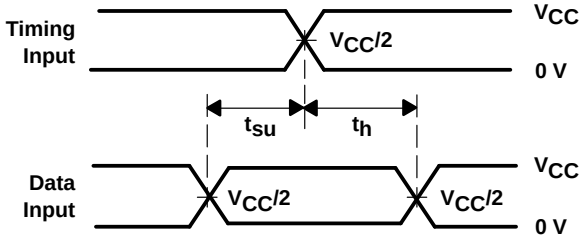


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

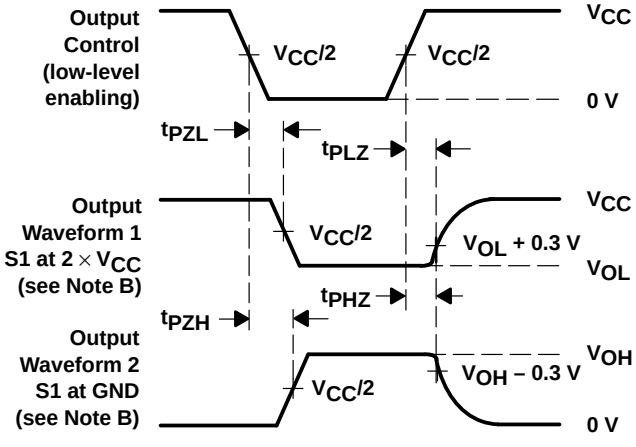
LOAD CIRCUIT



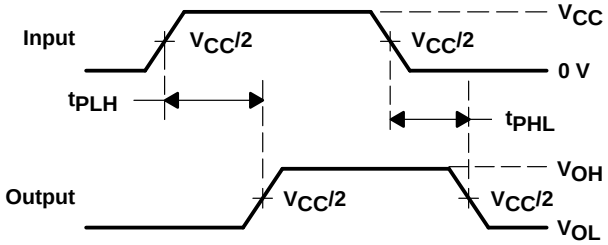
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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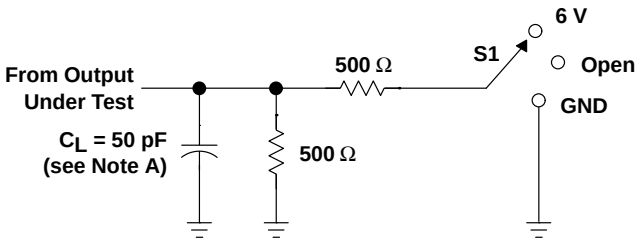
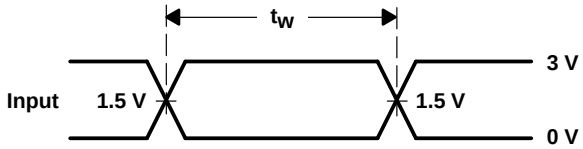
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3 V ± 0.3 V

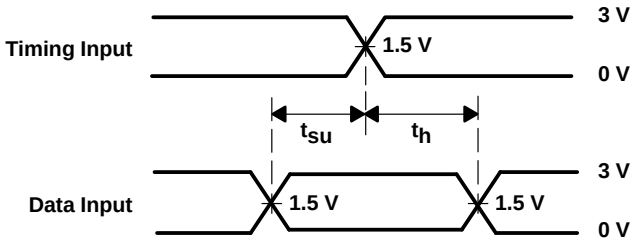


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

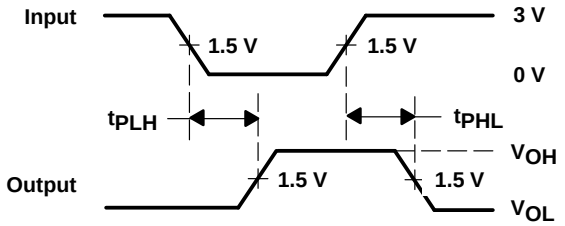
LOAD CIRCUIT



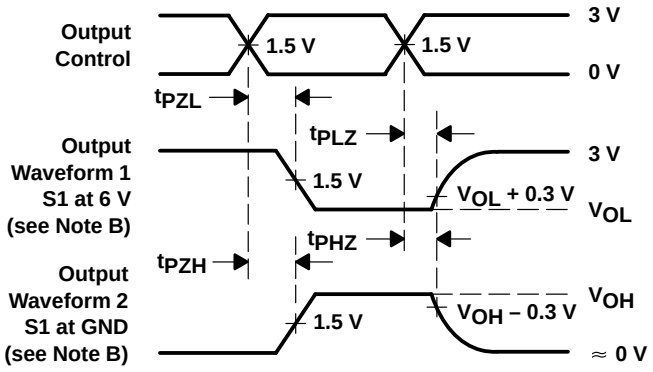
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

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