

SN54ALVTH16245, SN74ALVTH16245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES066A – JUNE 1996 – REVISED JULY 1996

- Members of the Texas Instruments *Widebus™* Family
- High-Impedance State During Power Up and Power Down
- 5-V I/O Compatible
- High-Drive Outputs (–32 mA/64 mA)
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Auto 3-State Eliminates Bus Current Loading When Voltage at the Output Exceeds V_{CC}
- Bus-Hold Data Inputs Eliminate the Need for External Pullup/Pulldown Resistors
- Power Off Disables Inputs/Outputs, Permitting Live Insertion
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package

description

The 'ALVTH16245 are 16-bit (dual-octal) noninverting 3-state transceivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

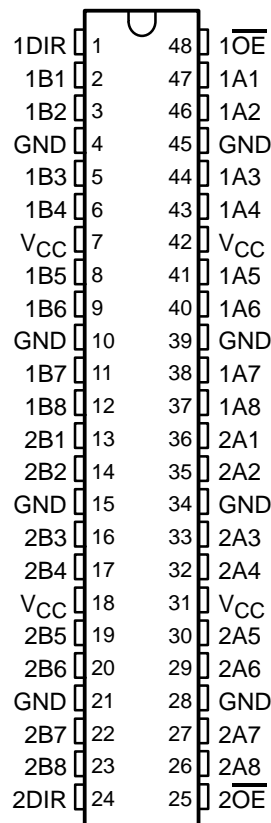
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVTH16245 is available in TI's thin very small-outline package (DGV), which provides the same I/O pin count and functionality of standard Widebus packages in less than half the printed circuit board area.

The SN54ALVTH16245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALVTH16245 is characterized for operation from -40°C to 85°C .

SN54ALVTH16245 . . . WD PACKAGE
SN74ALVTH16245 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW



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**TEXAS
INSTRUMENTS**

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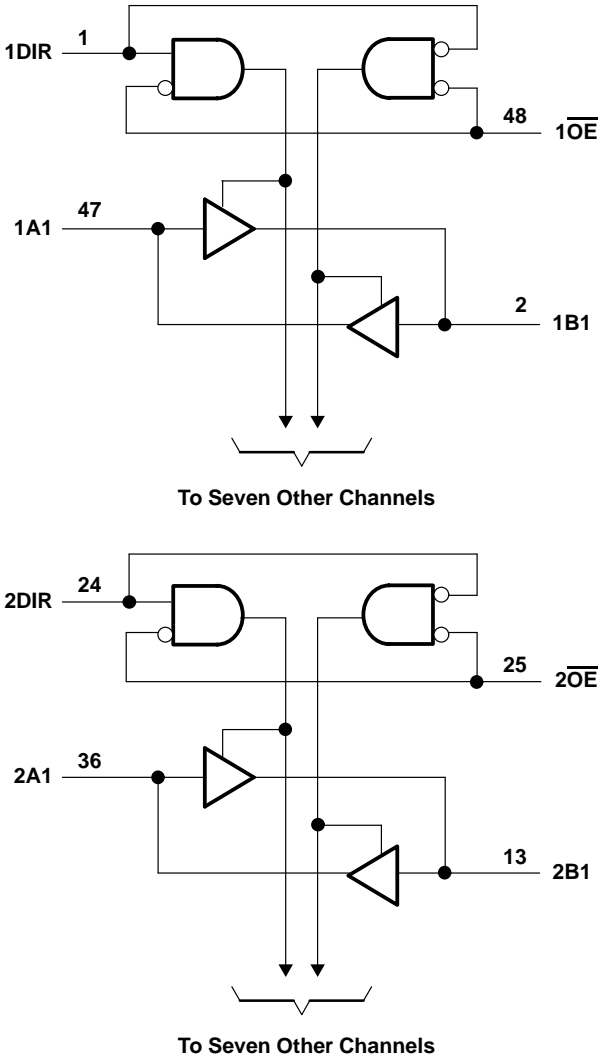
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FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output current in the low state, I_O : SN54ALVTH16245	96 mA
SN74ALVTH16245	128 mA
Output current in the high state, I_O : SN54ALVTH16245	–48 mA
SN74ALVTH16245	–64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package	0.85 W
DGV package	0.87 W
DL package	1.2 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (see Note 3)

		SN54ALVTH16245		SN74ALVTH16245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.3	2.7	2.3	2.7	V
V_{IH}	High-level input voltage	1.7		1.7		V
V_{IL}	Low-level input voltage		0.7		0.7	V
V_I	Input voltage	0	5.5	0	5.5	V
I_{OH}	High-level output current		–6		–8	mA
I_{OL}	Low-level output current		6		8	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ KHz}$		18		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

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recommended operating conditions, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (see Note 3)

			SN54ALVTH16245		SN74ALVTH16245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		3	3.6	3	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	5.5	0	5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			24		32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1 \text{ KHz}$			48		64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS		SN54ALVTH16245			SN74ALVTH16245			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}	V _{CC} = 2.3 V, I _I = −18 mA		−1.2			−1.2			V	
V _{OH}	V _{CC} = 2.3 V to 2.7 V, I _{OH} = −100 μA		V _{CC} −0.2			V _{CC} −0.2			V	
	V _{CC} = 2.3 V	I _{OH} = −6 mA	1.7							
		I _{OH} = −8 mA				1.7				
V _{OL}	V _{CC} = 2.3 V to 2.7 V, I _{OL} = 100 μA		0.2			0.2			V	
	V _{CC} = 2.3 V	I _{OL} = 6 mA	0.5							
		I _{OL} = 8 mA				0.5				
		I _{OL} = 18 mA	0.5							
		I _{OL} = 24 mA				0.5				
I _I	V _{CC} = 2.7 V, V _I = GND		±1			±1			μA	
	V _{CC} = 0 or 2.7 V, V _I = 2.7 V									
	V _{CC} = 2.7 V	V _I = V _{CC}	10			10				
		V _I = 0								10
V _{CC} = 0, V _I or V _O = 0 to 4.5 V		±100			±100			μA		
I _I (hold)	V _{CC} = 2.3 V	V _I = 0.7 V	90			90			μA	
		V _I = 1.7 V								75
	V _{CC} = 2.7 V‡, V _I = 0 to 2.7 V									
I _{EX} §	V _{CC} = 2.3 V, V _O = 3.6 V								μA	
I _{OZ} (PU/PD)¶	V _{CC} ≤ 1.2 V, V _I = GND or V _{CC} , V _O = 0.5 V to V _{CC} , $\overline{\text{OE}}$ = don't care		±100			±100			μA	
I _{CC}	V _{CC} = 2.7 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.04	0.09	0.04		0.09	mA
			Outputs low		2.3	4.5	2.3		4.5	
			Outputs disabled		0.04	0.09	0.04		0.09	
C _i	V _{CC} = 2.5 V, V _I = 2.5 V or 0		3			3			pF	
C _{io}	V _{CC} = 2.5 V, V _O = 2.5 V or 0		9			9			pF	

† All typical values are at $V_{CC} = 2.5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

§ Current into an output in the high state when $V_O > V_{CC}$

¶ High-impedance state during power up/high-impedance state during power down

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**electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 2)**

PARAMETER	TEST CONDITIONS		SN54ALVTH16245			SN74ALVTH16245			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$				-1.2			-1.2	V
V_{OH}	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2						
		$I_{OH} = -32\text{ mA}$				2			
V_{OL}	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$				0.2			0.2	V
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$						0.4	
		$I_{OL} = 24\text{ mA}$			0.5				
		$I_{OL} = 32\text{ mA}$						0.5	
		$I_{OL} = 48\text{ mA}$			0.55				
		$I_{OL} = 64\text{ mA}$						0.55	
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$	Control inputs			± 1			± 1	μA
	$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$				10			10	
	$V_{CC} = 3.6\text{ V}$	$V_I = 5.5\text{ V}$			20			20	
		$V_I = V_{CC}$			10			10	
		$V_I = 0$			-5			-5	
I_{off}	$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$				± 100			± 100	μA
$I_{I(hold)}$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$		75			75		μA
		$V_I = 2\text{ V}$		-75			-75		
	$V_{CC} = 3.6\text{ V}^\ddagger$, $V_I = 0\text{ to } 3.6\text{ V}$			± 500			± 500		
I_{EX}^\S	$V_{CC} = 3\text{ V}$, $V_O = 5.5\text{ V}$				125			125	μA
$I_{OZ(PU/PD)}^\P$	$V_{CC} \leq 1.2\text{ V}$, $V_I = \text{GND or } V_{CC}$, $V_O = 0.5\text{ V to } V_{CC}$, $OE = \text{don't care}$				± 100			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.07	0.09		0.07	0.09	mA
		Outputs low		3.2	5		3.2	5	
		Outputs disabled		0.07	0.09		0.07	0.09	
$\Delta I_{CC}^\#$	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC}-0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$				0.2			0.2	mA
C_i	$V_{CC} = 3.3\text{ V}$, $V_I = 3.3\text{ V or } 0$				3			3	pF
C_{io}	$V_{CC} = 3.3\text{ V}$, $V_O = 3.3\text{ V or } 0$				9			9	pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

§ Current into an output in the high state when $V_O > V_{CC}$

¶ High-impedance state during power up/high-impedance state during power down

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF, $V_{CC} = 2.5$ V \pm 0.2 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16245		SN74ALVTH16245			UNIT
			MIN	MAX	MIN	TYP†	MAX	
t_{pd}	A or B	B or A	1	3.9	1	2.3	3.5	ns
t_{en}	\overline{OE}	A or B	1.5	5.8	1.5	3.4	5.2	ns
t_{dis}	\overline{OE}	A or B	2	6.5	2	5.2	5.9	ns

† All typical values are at $V_{CC} = 2.5$ V, $T_A = 25^\circ\text{C}$.

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF, $V_{CC} = 3.3$ V \pm 0.3 V (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16245		SN74ALVTH16245			UNIT
			MIN	MAX	MIN	TYP‡	MAX	
t_{pd}	A or B	B or A	0.5	2.7	0.5	1.5	2.4	ns
t_{en}	\overline{OE}	A or B	1	4.2	1	2.4	3.8	ns
t_{dis}	\overline{OE}	A or B	1.5	5	1.5	3.8	4.5	ns

‡ All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

skew data

t_{ps} (pin skew or transition skew), $|t_{ps}| = 1 t_{PHL} - t_{PHL}$

t_{ps} max	$V_{CC} = 2.5$ V	$V_{CC} = 3.3$ V	UNIT
	469	267	ps

$t_{OST} = |t_{p\Phi m} - t_{p\Phi n}|$, where Φ is any edge transition (high to low or low to high) measured between any two outputs (m or n) within any given device

t_{OST}		$V_{CC} = 2.5$ V	$V_{CC} = 3.3$ V	UNIT
	A–B	625	427	ps
	B–A	547	427	

NOTE: One output switching, $T_A = 25^\circ\text{C}$

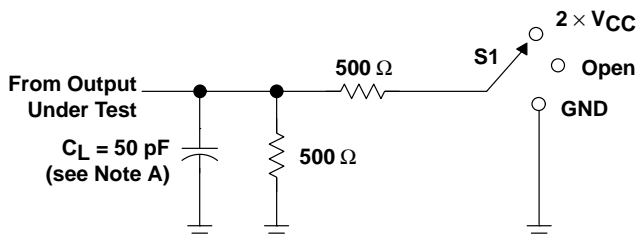
t_{OSHL}, t_{OSLH} , (common edge skew), $t_{OSHL} = |t_{PHL\max} - t_{PHL\min}|$ (output skew for low-to-high transitions), and $t_{OSLH} = |t_{PLH\max} - t_{PLH\min}|$ (output skew for high-to-low transitions)

		$V_{CC} = 2.5$ V	$V_{CC} = 3.3$ V	UNIT
t_{OSLH}	A–B	312	267	ps
t_{OSHL}	A–B	352	289	
t_{OSLH}	B–A	273	296	
t_{OSHL}	B–A	235	287	

NOTE: One output switching, $T_A = 25^\circ\text{C}$

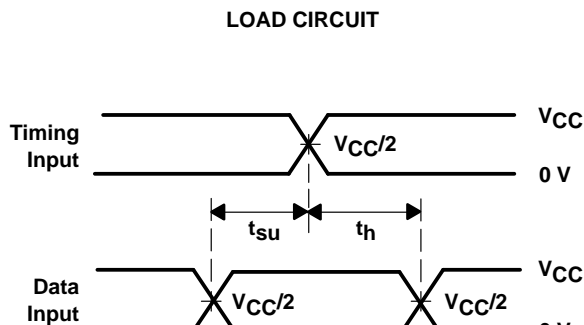
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

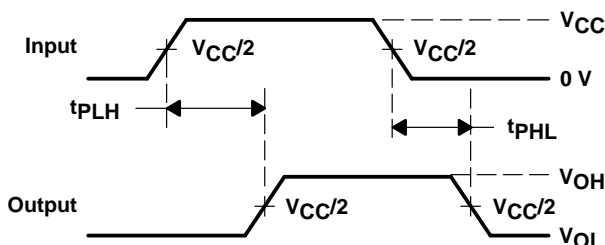


LOAD CIRCUIT

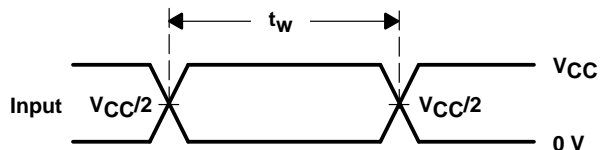
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



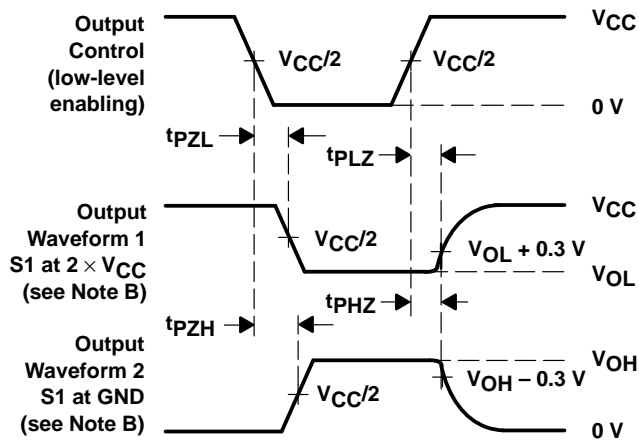
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

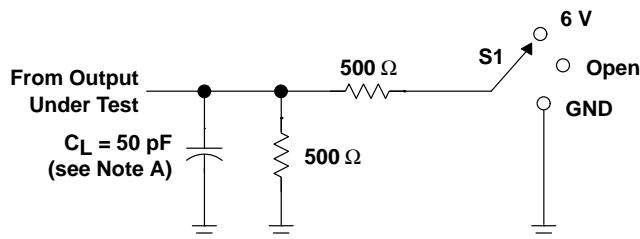
Figure 1. Load Circuit and Voltage Waveforms

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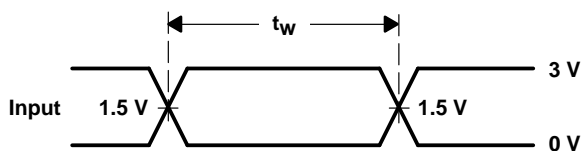
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$$

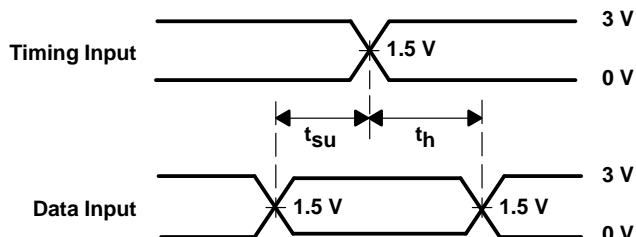


LOAD CIRCUIT

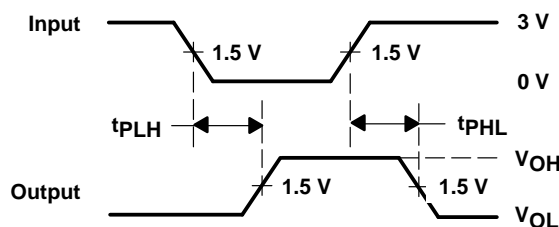
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



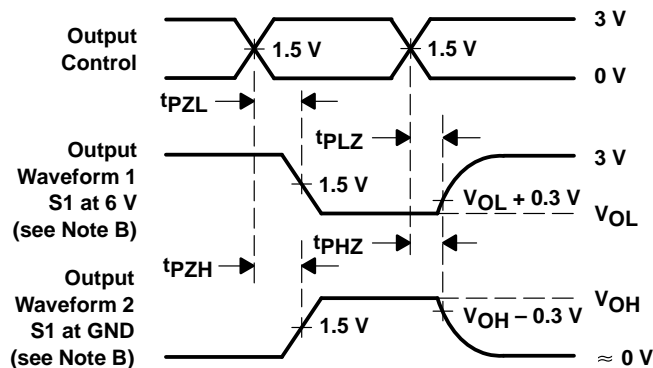
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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