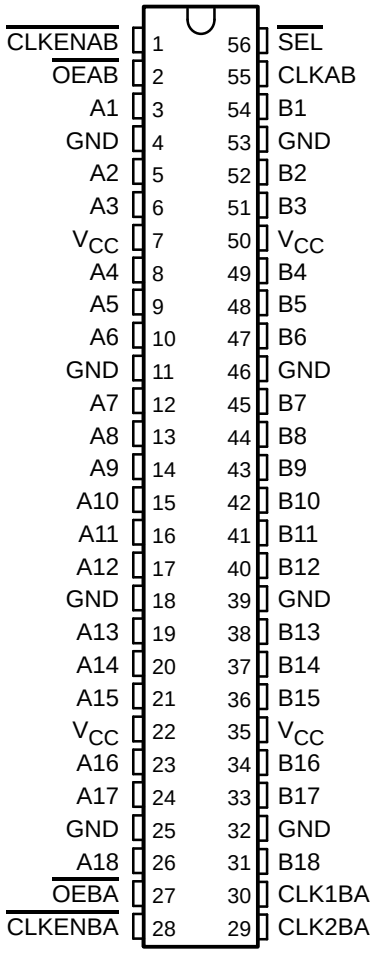
- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015;Exceeds 200V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Option Includes Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

**DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V $V_{CC}$ operation.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of $\overline{SEL}$.

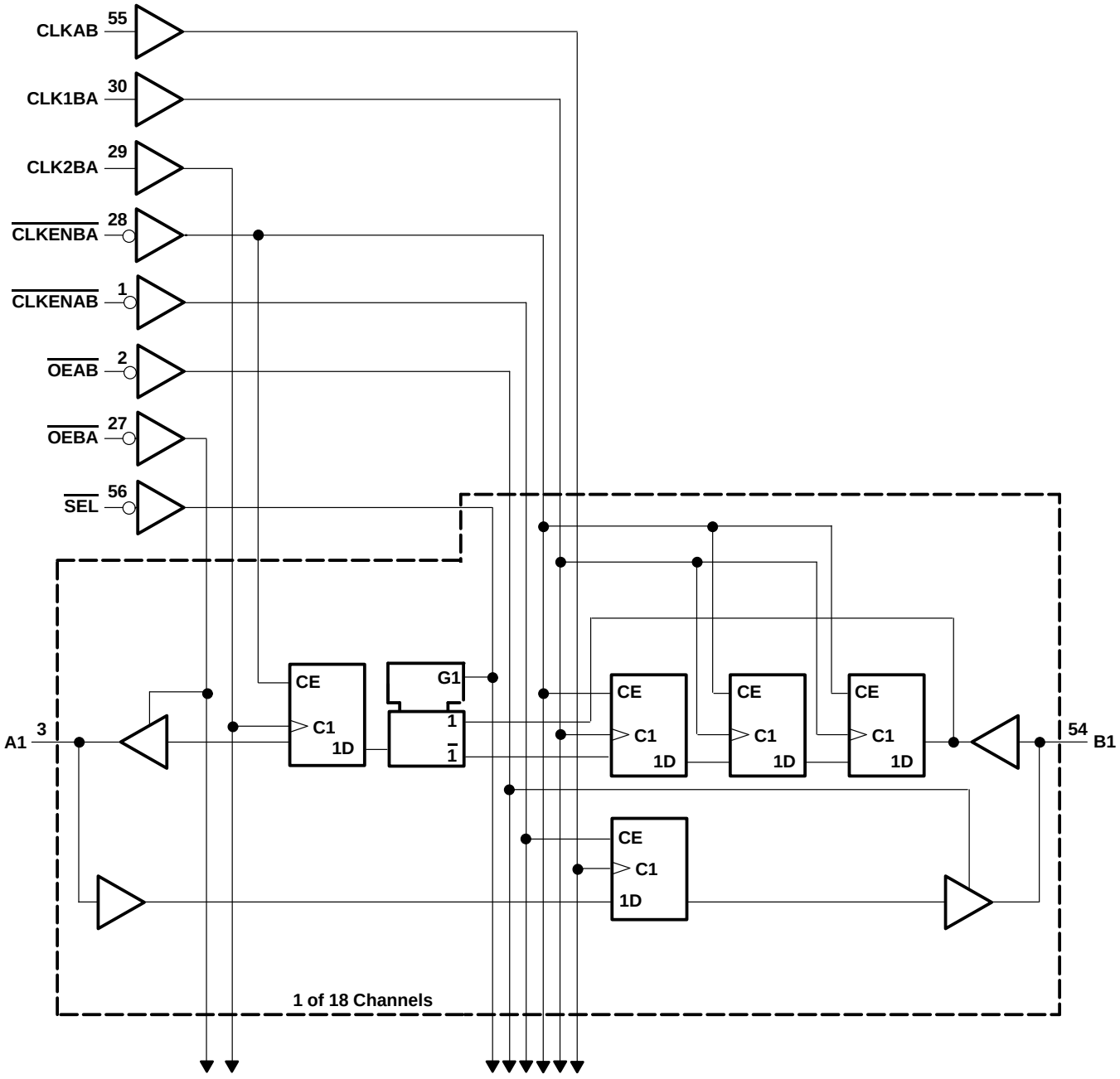
Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate $\overline{CLKEN}$ inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16525 is characterized for operation from –40°C to 85°C.

## logic diagram (positive logic)



## Function Tables

**A-TO-B STORAGE ($\overline{OEAB}$ = L)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{CLKENAB}$ | CLKAB | A | B |
| H | X | X | $B_0$† |
| L | ↑ | L | L |
| L | ↑ | H | H |

† Output level before the indicated steady-state input conditions were established

**B-TO-A STORAGE ($\overline{OEBA}$ = L)**

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| $\overline{CLKENBA}$ | CLK2BA | CLK1BA | $\overline{SEL}$ | B | A |
| H | X | X | X | X | $A_0$† |
| L | ↑ | X | H | L | L |
| L | ↑ | X | H | H | H |
| L | ↑ | ↑ | L | L | L‡ |
| L | ↑ | ↑ | L | H | H‡ |

† Output level before the indicated steady-state input conditions were established

‡ Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when $\overline{SEL}$ is low.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 4.6 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±100 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

## recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.3 V | | –12 | mA |
| | | $V_{CC}$ = 2.7 V | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.3 V | | 12 | mA |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –100 μA | | 2.3 V to 3.6 V | $V_{CC}$–0.2 | | | V |
| | | $I_{OH}$ = –6 mA, | $V_{IH}$ = 1.7 V | 2.3 V | 2 | | | |
| | | $I_{OH}$ = –12 mA | $V_{IH}$ = 1.7 V | 2.3 V | 1.7 | | | |
| | | | $V_{IH}$ = 2 V | 2.7 V | 2.2 | | | |
| | | | $V_{IH}$ = 2 V | 3 V | 2.4 | | | |
| | | $I_{OH}$ = –24 mA, | $V_{IH}$ = 2 V | 3 V | 2 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA | | 2.3 V to 3.6 V | | | 0.2 | V |
| | | $I_{OL}$ = 6 mA, | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.4 | |
| | | $I_{OL}$ = 12 mA | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.7 | |
| | | | $V_{IL}$ = 0.8 V | 2.7 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA, | $V_{IL}$ = 0.8 V | 3 V | | | 0.55 | |
| $I_I$ | | $V_I$ = $V_{CC}$ or GND | | 3.6 V | | | ±5 | μA |
| $I_{hold}$ | | $V_I$ = 0.7 V | | 2.3 V | 45 | | | μA |
| | | $V_I$ = 1.7 V | | | –45 | | | |
| | | $V_I$ = 0.8 V | | 3 V | 75 | | | |
| | | $V_I$ = 2 V | | | –75 | | | |
| | | $V_I$ = 0 to 3.6 V‡ | | 3.6 V | | | ±500 | |
| $I_{OZ}$§ | | $V_O$ = $V_{CC}$ or GND | | 3.6 V | | | ±10 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 3.6 V | | | 40 | μA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ – 0.6 V, | Other inputs at $V_{CC}$ or GND | 3 V to 3.6 V | | | 750 | μA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 3 | | pF |
| $C_o$ | A or B ports | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 7 | | pF |

† All typical values are at $V_{CC}$ = 3.3, $T_A$ = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter $I_{OZ}$ includes the input-leakage current.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)**

| | | | $V_{CC}$ = 2.5 V ±0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 120 | 0 | 125 | 0 | 150 | MHz |
| $t_w$ | Pulse duration, CLK high or low | | 3.2 | | 3.2 | | 3 | | ns |
| $t_{su}$ | Setup time | A data before CLKAB↑ | 1.3 | | 1.3 | | 1.3 | | ns |
| | | B data before CLK2BA↑ | 2.1 | | 1.8 | | 1.7 | | |
| | | B data before CLK1BA↑ | 1.3 | | 1.2 | | 1.1 | | |
| | | $\overline{SEL}$ before CLK2BA↑ | 3.3 | | 3.3 | | 3.3 | | |
| | | $\overline{CLKENAB}$ before CLKAB↑ | 2.1 | | 1.9 | | 1.6 | | |
| | | $\overline{CLKENBA}$ before CLK1BA↑ | 2.7 | | 2.5 | | 2.1 | | |
| | | $\overline{CLKENBA}$ before CLK2BA↑ | 2.7 | | 2.5 | | 2.2 | | |
| $t_h$ | Hold time | A data after CLKAB↑ | 0.7 | | 0.4 | | 0.9 | | ns |
| | | B data after CLK2BA↑ | 0.4 | | 0 | | 0.6 | | |
| | | B data after CLK1BA↑ | 0.8 | | 0.4 | | 1 | | |
| | | $\overline{SEL}$ after CLK2BA↑ | 0 | | 0 | | 0.1 | | |
| | | $\overline{CLKENAB}$ after CLKAB↑ | 0.1 | | 0.3 | | 0.3 | | |
| | | $\overline{CLKENBA}$ after CLK1BA↑ | 0 | | 0 | | 0.1 | | |
| | | $\overline{CLKENBA}$ after CLK2BA↑ | 0 | | 0 | | 0 | | |

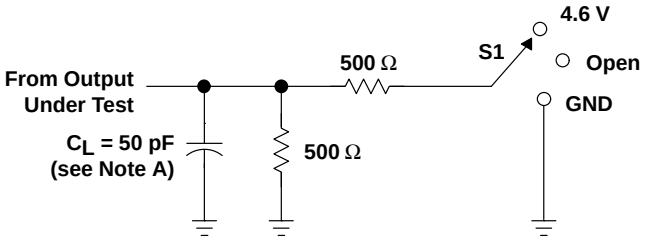
**switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figures 1 and 2)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 120 | | 125 | | 150 | | MHz |
| $t_{pd}$ | CLKAB or CLK2BA | A or B | 1 | 5.1 | | 4.4 | 1 | 4.2 | ns |
| $t_{en}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | A or B | 1 | 6.6 | | 6.1 | 1 | 5.1 | ns |
| $t_{dis}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | A or B | 1 | 6.5 | | 5.4 | 1 | 4.9 | ns |

**operating characteristics, $T_A$ = 25°C**

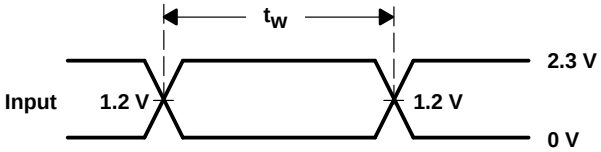
| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V | UNIT |
|---|---|---|---|---|---|---|
| | | | | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, f = 10 MHz | 160 | 160 | pF |
| | | Outputs disabled | | | | |

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

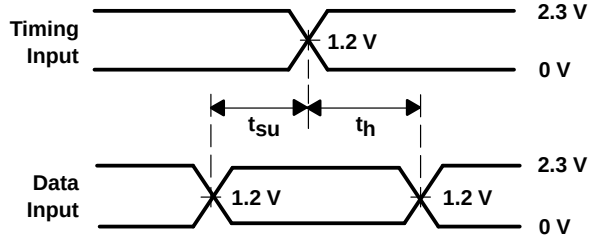



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 4.6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

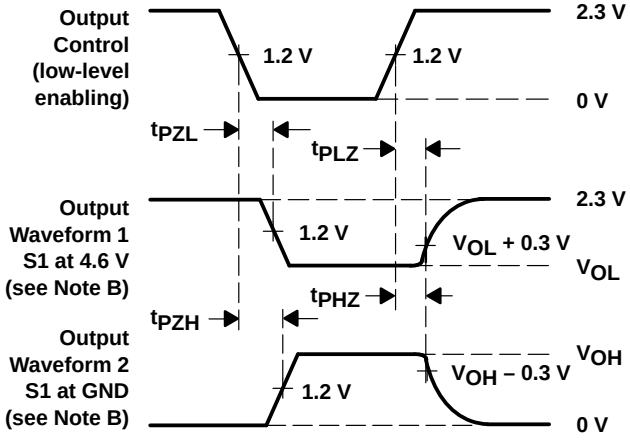
LOAD CIRCUIT



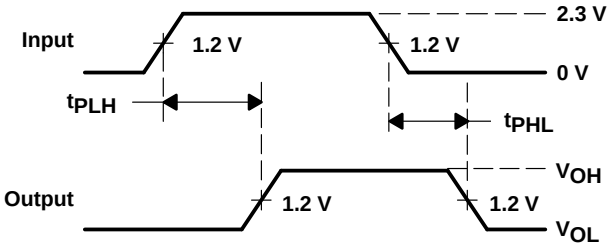

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

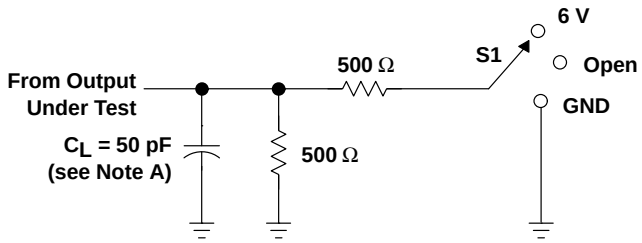



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

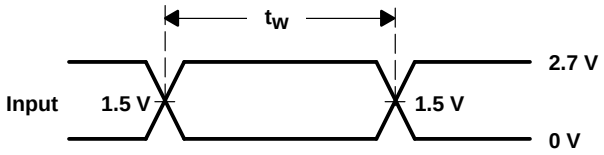
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.7 V AND 3.3 V ± 0.3 V

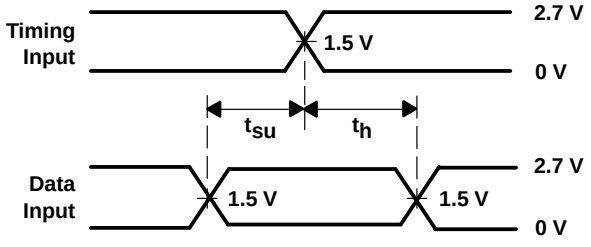



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

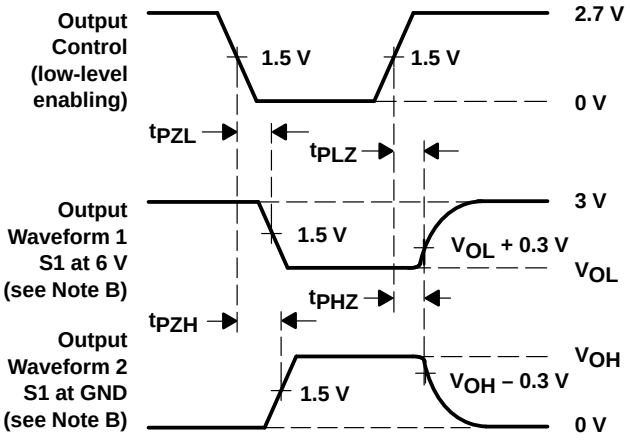
LOAD CIRCUIT



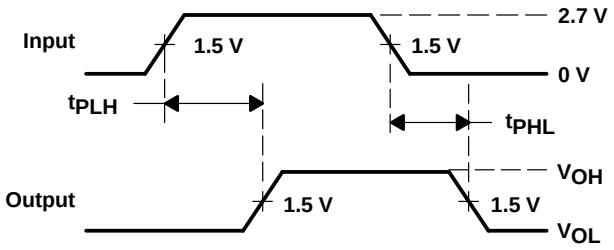

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 2. Load Circuit and Voltage Waveforms**

## IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.