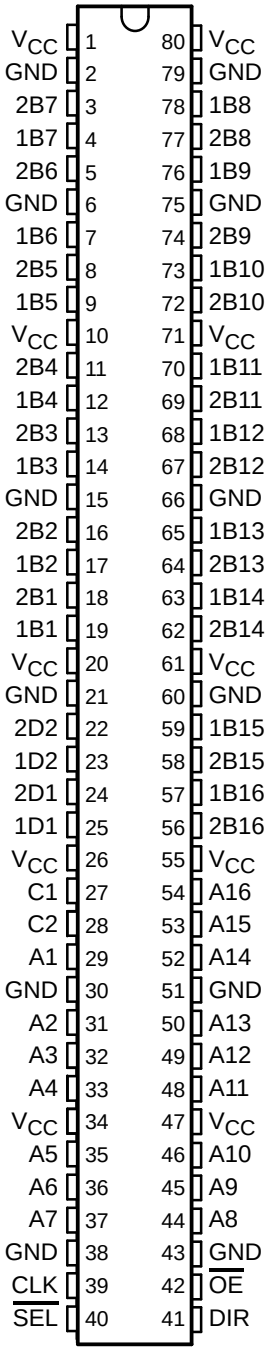
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Member of the Texas Instruments Widebus™ Family**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Thin Shrink Small-Outline Package**

DBB PACKAGE
(TOP VIEW)



description

This 16-bit to 32-bit registered bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation. This device is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

The device provides synchronous data exchange between the A and B ports. Data is stored in the internal registers on the low-to-high transition of the CLK input. For data transfer in the B to A direction, $\overline{SEL}$ selects 1B or 2B data for the A outputs.

For data transfer in the A to B direction, a two stage pipeline is provided in the 1B path, and a single storage register in the 2B path. Data flow is controlled by the active-low output enable ($\overline{OE}$) and the DIR input. The DIR control pin is registered to synchronize the bus direction changes with the clock.

Two mask bits are provided for both data bytes. The D outputs are controlled by the active-low $\overline{OE}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16280 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

Function Tables

OUTPUT ENABLE

INPUTS			OUTPUTS		
CLK	$\overline{OE}$	DIR	A	1B, 2B	1D, 2D
↑	H	X	Z	Z	Z
↑	L	H	Z	Active	Active
↑	L	L	Active	Z	Active

A-TO-B STORAGE ($\overline{OE}$ = L, DIR = H)

INPUTS			OUTPUTS	
$\overline{SEL}$	CLK	A	1B	2B
H	X	X	$1B_0$†	$2B_0$†
L	↑	L	L‡	L
L	↑	H	H‡	H

† Output level before the indicated steady-state input conditions were established

‡ Two CLK edges are needed to propagate the data.

B-TO-A STORAGE ($\overline{OE}$ = L, DIR = L)

INPUTS				OUTPUT
CLK	$\overline{SEL}$	1B	2B	A
↑	H	X	L	L§
↑	H	X	H	H§
↑	L	L	X	L
↑	L	H	X	H

§ Two clock edges are needed to propagate the data. The data is loaded in the first register when $\overline{SEL}$ is low and propagates to the second register when $\overline{SEL}$ is high.

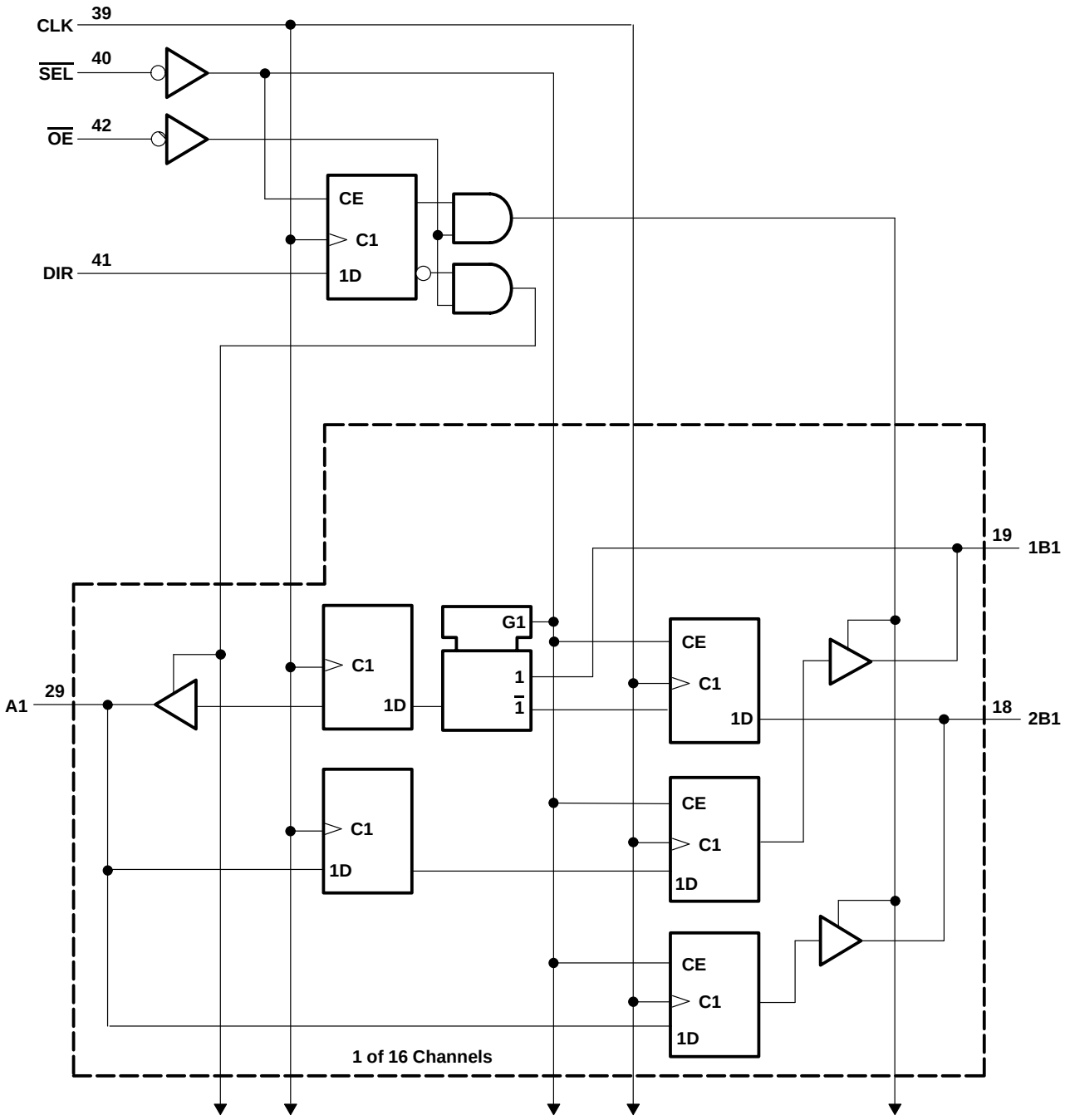
C-TO-D STORAGE ($\overline{OE}$ = L)

INPUTS			OUTPUTS	
$\overline{SEL}$	CLK	A	1B	2B
H	X	X	$1D_0$†	$2D_0$†
L	↑	L	L‡	L
L	↑	H	H‡	H

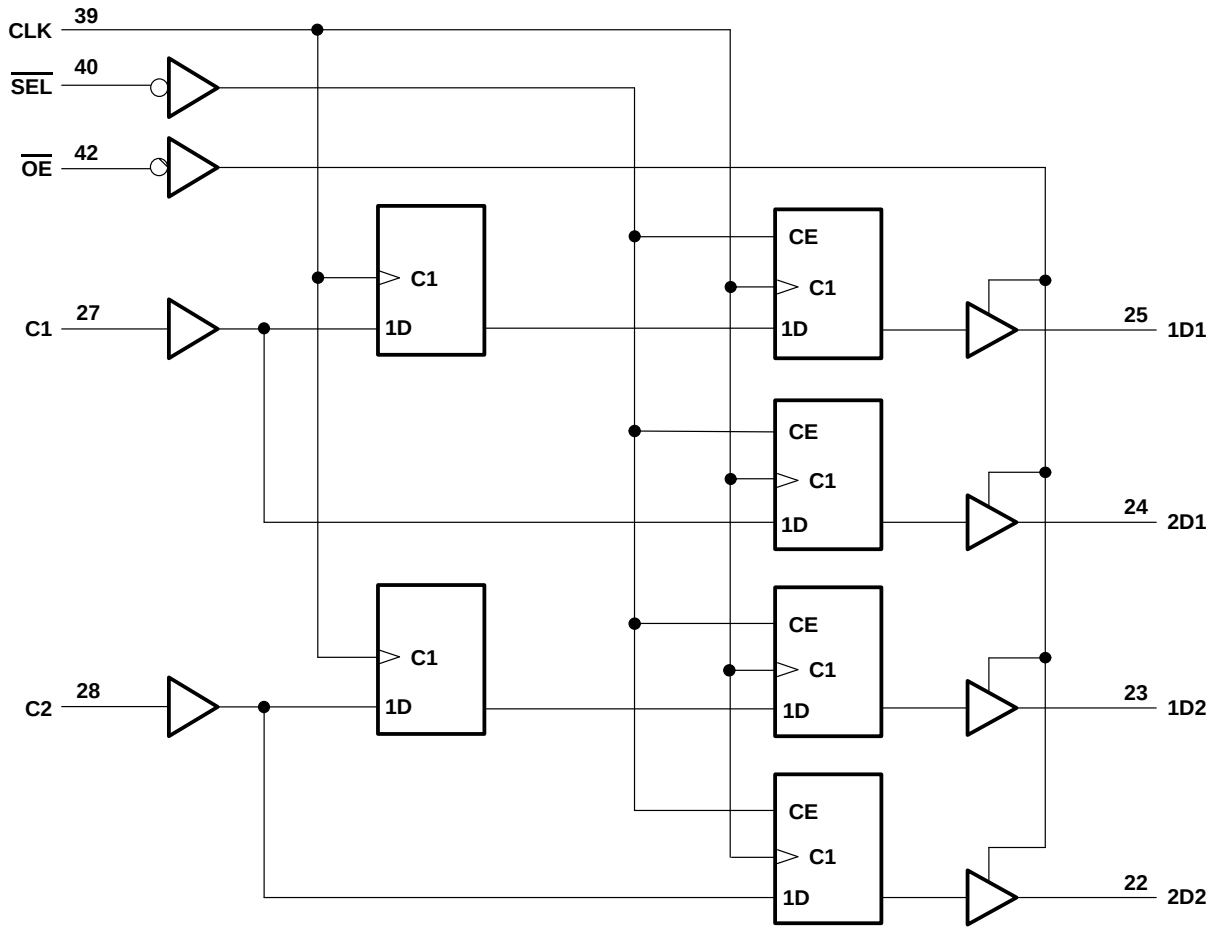
† Output level before the indicated steady-state input conditions were established

‡ Two CLK edges are needed to propagate the data.

logic diagram (positive logic)



logic diagram (positive logic) (mask bits)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I: Except I/O ports (see Note 1) . . . . . –0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3) . . . . . 0.8 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

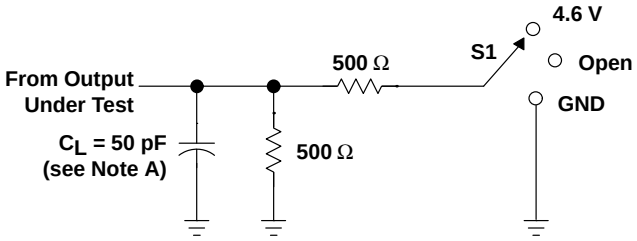
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	TYP‡	MAX	UNIT
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
	I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
		V_{IH} = 2 V	2.7 V	2.2			
		V_{IH} = 2 V	3 V	2.4			
	I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
	I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
		V_{IL} = 0.8 V	2.7 V			0.4	
	I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$	V_I = 0.7 V		2.3 V	45			µA
	V_I = 1.7 V			–45			
	V_I = 0.8 V		3 V	75			
	V_I = 2 V			–75			
	V_I = 0 to 3.6 V		3.6 V			±500	
I_{OZ}§	V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to3.6 V			750	µA
C_i	V_I = V_{CC} or GND		3.3 V				pF
C_{io}	V_O = V_{CC} or GND		3.3 V				pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

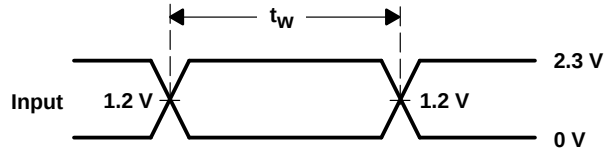
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

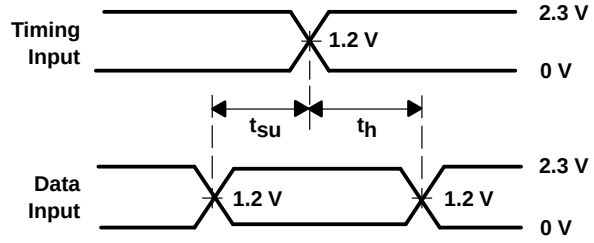


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

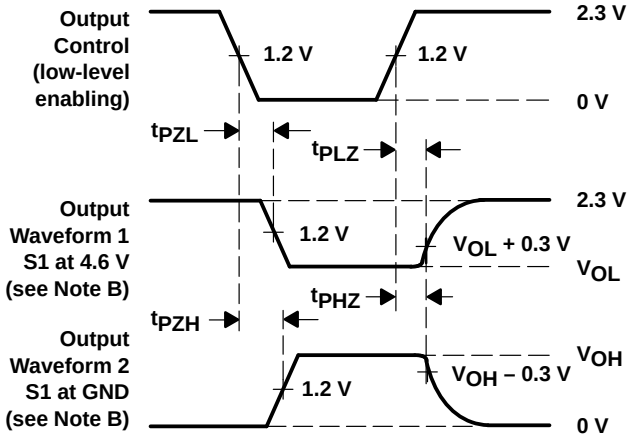
LOAD CIRCUIT



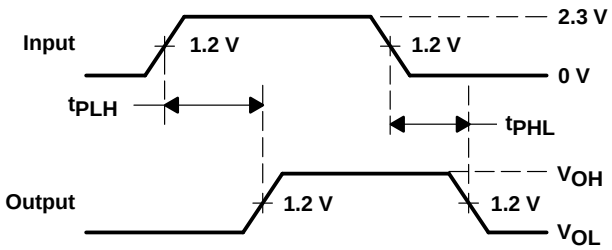
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



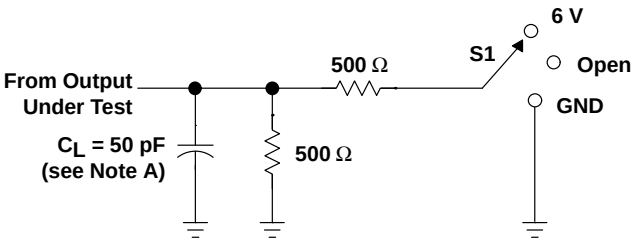
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

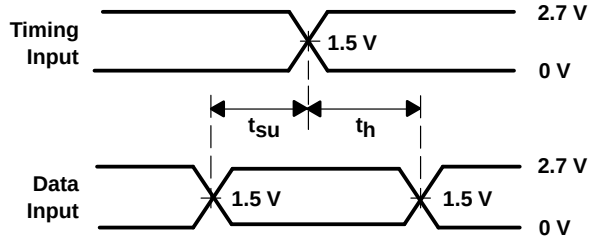
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

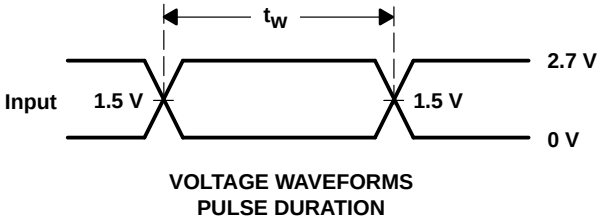


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

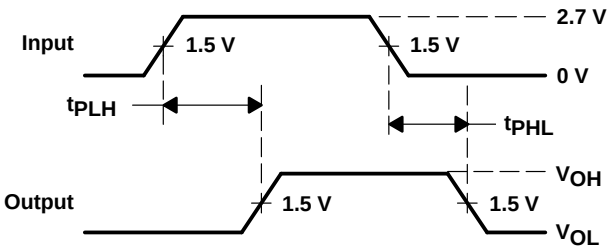
LOAD CIRCUIT



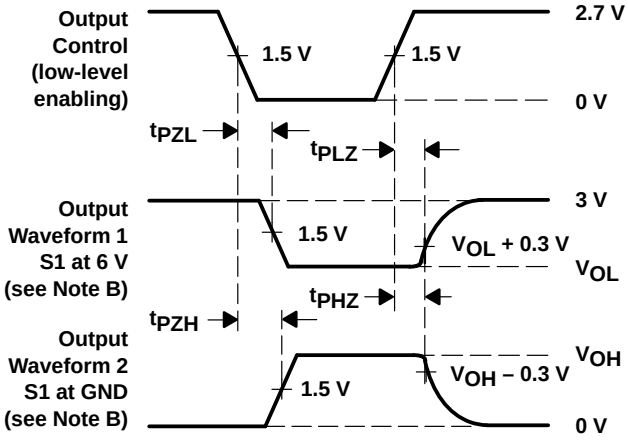
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

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