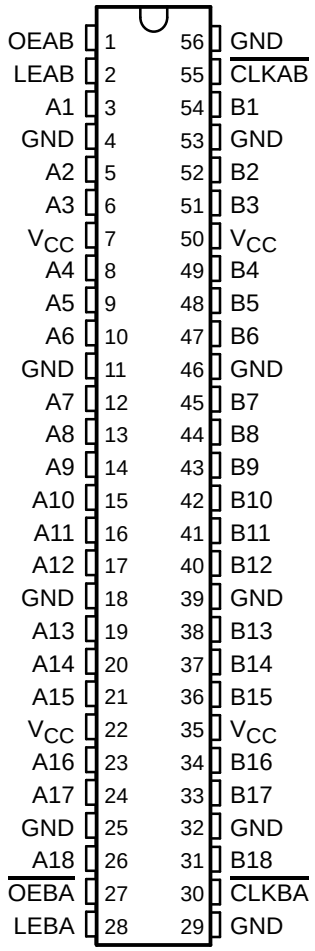
- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

**DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V $V_{CC}$ operation.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to $V_{CC}$ through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16500 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

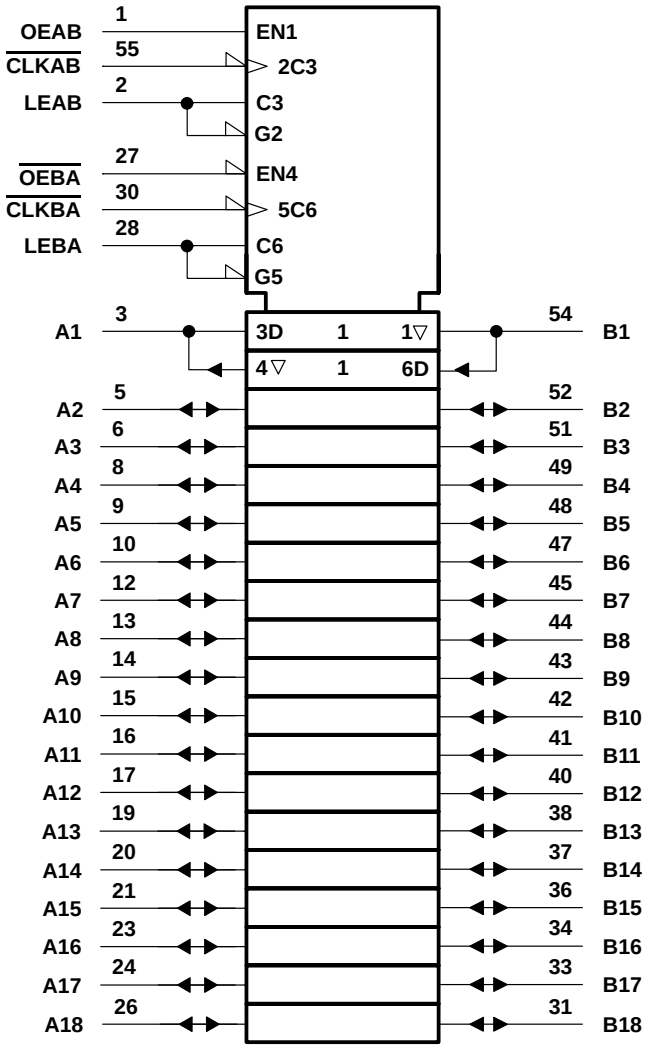
The SN74ALVCH16500 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE†**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| OEAB | LEAB | $\overline{\text{CLKAB}}$ | A | B |
| L | X | X | X | Z |
| H | H | X | L | L |
| H | H | X | H | H |
| H | L | ↓ | L | L |
| H | L | ↓ | H | H |
| H | L | H | X | $B_0$‡ |
| H | L | L | X | $B_0$§ |

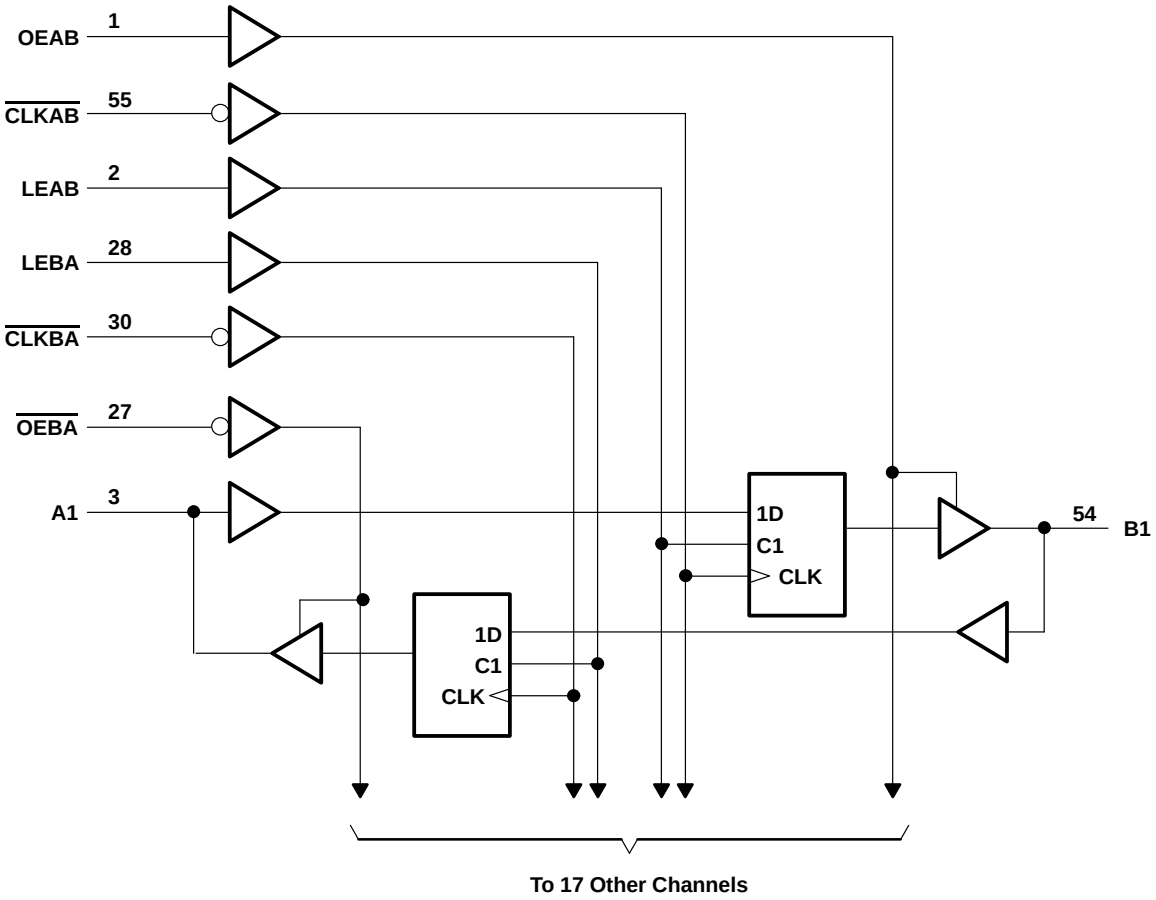
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.
‡ Output level before the indicated steady-state input conditions were established
§ Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low

## logic symbol¶




¶ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1) . . . . . –0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±100 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

## recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.3 V | | –12 | mA |
| | | $V_{CC}$ = 2.7 V | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.3 V | | 12 | mA |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –100 μA | | 2.3 V to 3.6 V | $V_{CC}$–0.2 | | | V |
| | | $I_{OH}$ = –6 mA, | $V_{IH}$ = 1.7 V | 2.3 V | 2 | | | |
| | | $I_{OH}$ = –12 mA | $V_{IH}$ = 1.7 V | 2.3 V | 1.7 | | | |
| | | | $V_{IH}$ = 2 V | 2.7 V | 2.2 | | | |
| | | | $V_{IH}$ = 2 V | 3 V | 2.4 | | | |
| | | $I_{OH}$ = –24 mA, | $V_{IH}$ = 2 V | 3 V | 2 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA | | 2.3 V to 3.6 V | | | 0.2 | V |
| | | $I_{OL}$ = 6 mA, | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.4 | |
| | | $I_{OL}$ = 12 mA | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.7 | |
| | | | $V_{IL}$ = 0.8 V | 2.7 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA, | $V_{IL}$ = 0.8 V | 3 V | | | 0.55 | |
| $I_I$ | | $V_I$ = $V_{CC}$ or GND | | 3.6 V | | | ±5 | μA |
| $I_{I(hold)}$ | | $V_I$ = 0.7 V | | 2.3 V | 45 | | | μA |
| | | $V_I$ = 1.7 V | | | –45 | | | |
| | | $V_I$ = 0.8 V | | 3 V | 75 | | | |
| | | $V_I$ = 2 V | | | –75 | | | |
| | | $V_I$ = 0 to 3.6 V‡ | | 3.6 V | | | ±500 | |
| $I_{OZ}$§ | | $V_O$ = $V_{CC}$ or GND | | 3.6 V | | | ±10 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 3.6 V | | | 40 | μA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ – 0.6 V, | Other inputs at $V_{CC}$ or GND | 3 V to 3.6 V | | | 750 | μA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 4 | | pF |
| $C_{io}$ | A or B ports | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 8 | | pF |

† Typical values are measured at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

### timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 150 | 0 | 150 | 0 | 150 | MHz |
| $t_w$ | Pulse duration | LE high | 3.3 | | 3.3 | | 3.3 | | ns |
| | | $\overline{CLK}$ high or low | 3.3 | | 3.3 | | 3.3 | | |
| $t_{su}$ | Setup time | Data before $\overline{CLK}\downarrow$ | 1.7 | | 1.4 | | 1.3 | | ns |
| | | Data before LE↓, $\overline{CLK}$ high | 1.1 | | 1 | | 1 | | |
| | | Data before LE↓, $\overline{CLK}$ low | 1.9 | | 1.6 | | 1.4 | | |
| $t_h$ | Hold time | Data after $\overline{CLK}\downarrow$ | 1.7 | | 1.6 | | 1.3 | | ns |
| | | Data after LE↓, $\overline{CLK}$ high | 2 | | 1.8 | | 1.5 | | |
| | | Data after LE↓, $\overline{CLK}$ low | 1.6 | | 1.5 | | 1.2 | | |

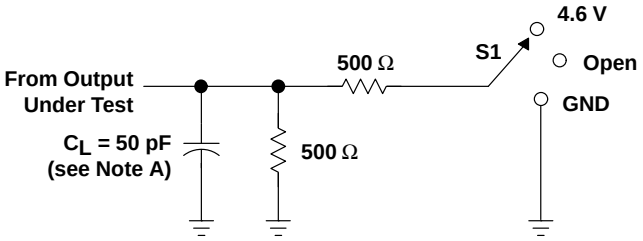
### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 150 | | 150 | | 150 | | MHz |
| $t_{pd}$ | A or B | B or A | 1 | 5.7 | | 4.7 | 1 | 3.9 | ns |
| | LEAB or LEBA | A or B | 1 | 6.5 | | 5.5 | 1 | 4.7 | |
| | $\overline{CLKAB}$ or $\overline{CLKBA}$ | A or B | 1 | 7.2 | | 6.6 | 1.1 | 5.5 | |
| $t_{en}$ | OEAB | B | 1 | 6.2 | | 5.4 | 1 | 4.6 | ns |
| $t_{dis}$ | OEAB | B | 1.7 | 6.3 | | 5.7 | 1.5 | 5 | ns |
| $t_{en}$ | $\overline{OEBA}$ | A | 1 | 6.7 | | 6.2 | 1 | 5.2 | ns |
| $t_{dis}$ | $\overline{OEBA}$ | A | 1 | 5.6 | | 4.6 | 1 | 4.3 | ns |

### operating characteristics, $T_A$ = 25°C

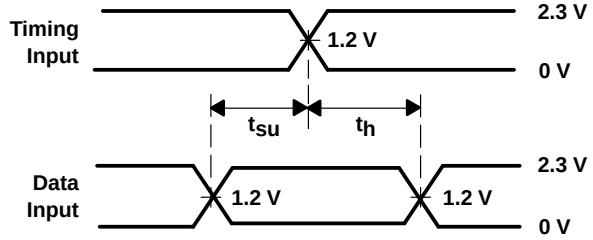
| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V | UNIT |
|---|---|---|---|---|---|---|
| | | | | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, f = 10 MHz | 40 | 51 | pF |
| | | Outputs disabled | | 6 | 6 | |

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

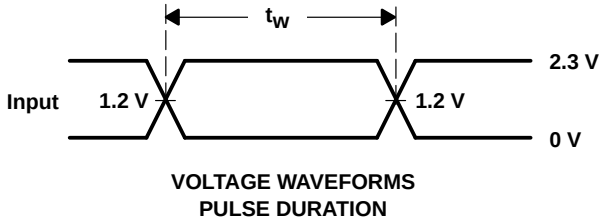



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 4.6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

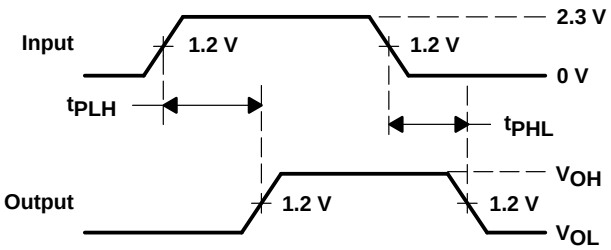
LOAD CIRCUIT



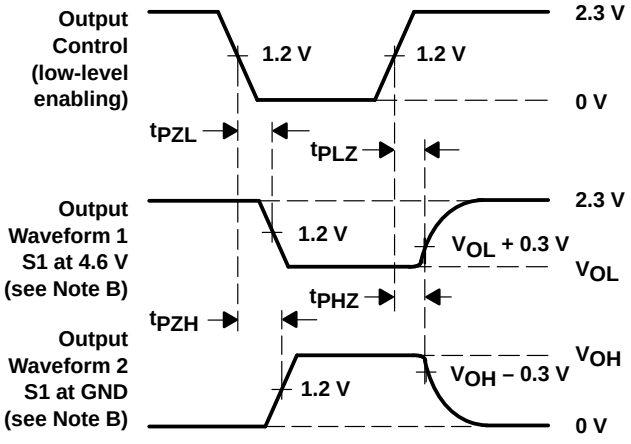

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

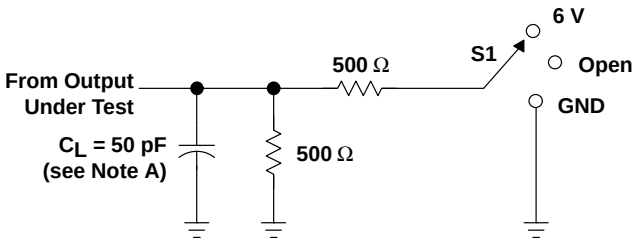



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

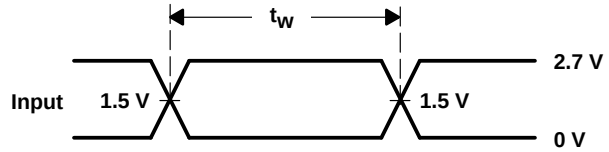
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.7 V AND 3.3 V ± 0.3 V

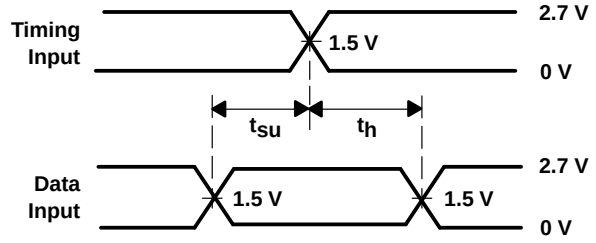



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

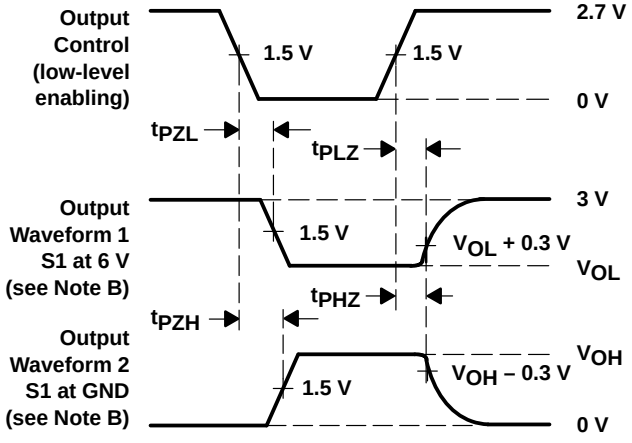
LOAD CIRCUIT



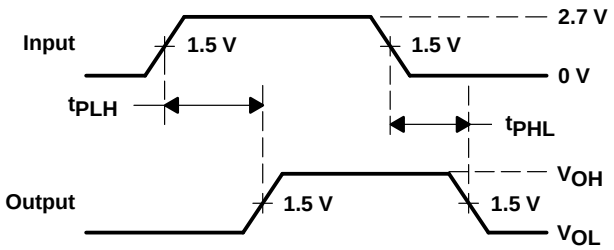

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 2. Load Circuit and Voltage Waveforms**

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