

# SN74ALVCH162827

## 20-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

SCES013B – JULY 1995 – REVISED DECEMBER 1996

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

#### description

This 20-bit noninverting buffer/driver is designed for 2.3-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH162827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ( $\overline{1OE1}$  and  $\overline{1OE2}$  or  $\overline{2OE1}$  and  $\overline{2OE2}$ ) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162827 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH162827 is characterized for operation from -40°C to 85°C.

#### DGG OR DL PACKAGE (TOP VIEW)

$\overline{1OE1}$	1	56	$\overline{1OE2}$
1Y1	2	55	1A1
1Y2	3	54	1A2
GND	4	53	GND
1Y3	5	52	1A3
1Y4	6	51	1A4
$V_{CC}$	7	50	$V_{CC}$
1Y5	8	49	1A5
1Y6	9	48	1A6
1Y7	10	47	1A7
GND	11	46	GND
1Y8	12	45	1A8
1Y9	13	44	1A9
1Y10	14	43	1A10
2Y1	15	42	2A1
2Y2	16	41	2A2
2Y3	17	40	2A3
GND	18	39	GND
2Y4	19	38	2A4
2Y5	20	37	2A5
2Y6	21	36	2A6
$V_{CC}$	22	35	$V_{CC}$
2Y7	23	34	2A7
2Y8	24	33	2A8
GND	25	32	GND
2Y9	26	31	2A9
2Y10	27	30	2A10
$\overline{2OE1}$	28	29	$\overline{2OE2}$



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

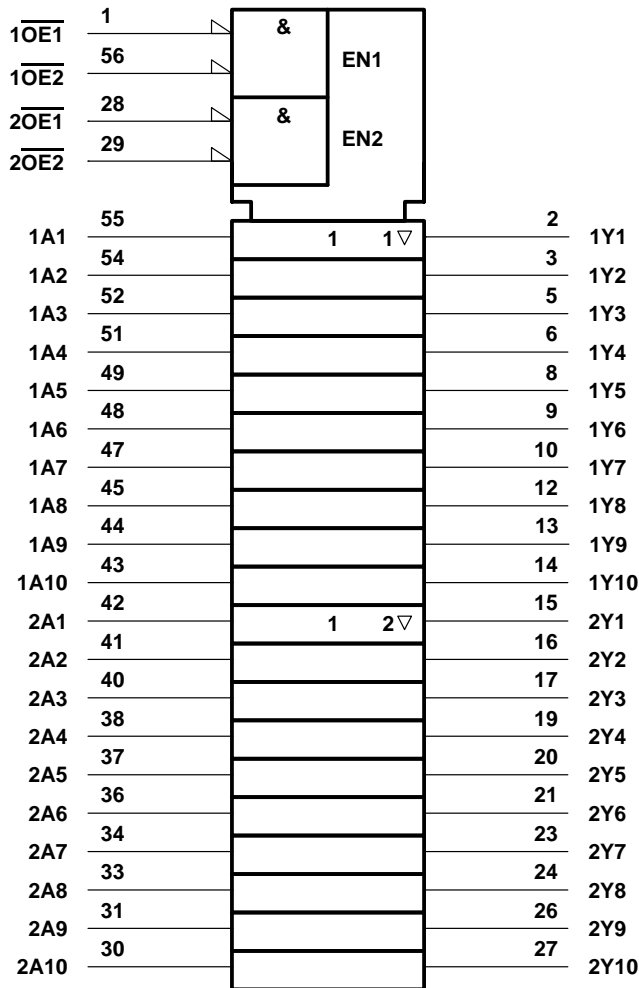
Copyright © 1996, Texas Instruments Incorporated

FUNCTION TABLE

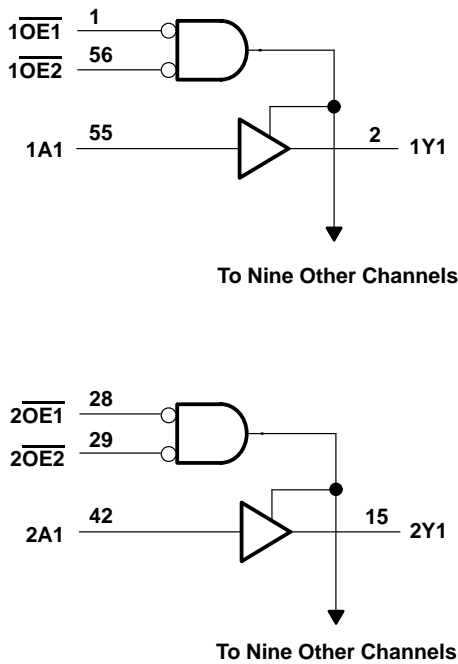
(each 10-bit section)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 4.6 V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1.4 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This value is limited to 4.6 V maximum.
  3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

**recommended operating conditions (see Note 4)**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2.3	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	1.7		V
		$V_{CC} = 2.7$ V to 3.6 V	2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.3$ V to 2.7 V		0.7	V
		$V_{CC} = 2.7$ V to 3.6 V		0.8	
$V_I$	Input voltage		0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.3$ V		–6	mA
		$V_{CC} = 2.7$ V		–8	
		$V_{CC} = 3$ V		–12	
$I_{OL}$	Low-level output current	$V_{CC} = 2.3$ V		6	mA
		$V_{CC} = 2.7$ V		8	
		$V_{CC} = 3$ V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
$T_A$	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

**SN74ALVCH162827**  
**20-BIT BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

SCES013B – JULY 1995 – REVISED DECEMBER 1996

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2			V
	I <sub>OH</sub> = -4 mA, V <sub>IH</sub> = 1.7 V		2.3 V	1.9			
	I <sub>OH</sub> = -6 mA	V <sub>IH</sub> = 1.7 V	2.3 V	1.7			
		V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>OH</sub> = -8 mA, V <sub>IH</sub> = 2 V		2.7 V	2			
	I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2 V		3 V	2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA		2.3 V to 3.6 V			0.2	V
	I <sub>OL</sub> = 4 mA, V <sub>IL</sub> = 0.7 V		2.3 V			0.4	
	I <sub>OL</sub> = 6 mA	V <sub>IL</sub> = 0.7 V	2.3 V			0.55	
		V <sub>IL</sub> = 0.8 V	3 V			0.55	
	I <sub>OL</sub> = 8 mA, V <sub>IL</sub> = 0.8 V		2.7 V			0.6	
	I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V		3 V			0.8	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V			±5	μA
I <sub>I</sub> (hold)	V <sub>I</sub> = 0.7 V		2.3 V	45			μA
	V <sub>I</sub> = 1.7 V			-45			
	V <sub>I</sub> = 0.8 V		3 V	75			
	V <sub>I</sub> = 2 V			-75			
	V <sub>I</sub> = 0 to 3.6 V‡		3.6 V			±500	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		3.6 V			40	μA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3.5			pF
	Data inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	6			pF
C <sub>O</sub>	Outputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	7			pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figures 1 and 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	1.3	5	4.4		1.5	3.8	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y	1.5	6.8	6.2		1.6	5.1	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	2.4	6.1	5.2		1.8	4.7	ns

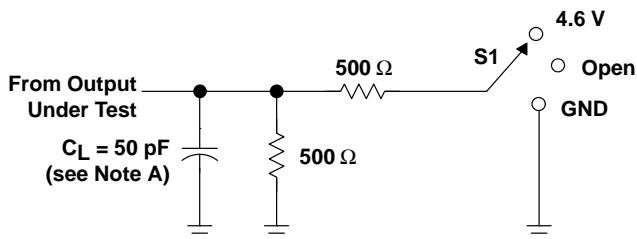
**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	16	18	pF
		Outputs disabled	4	6	



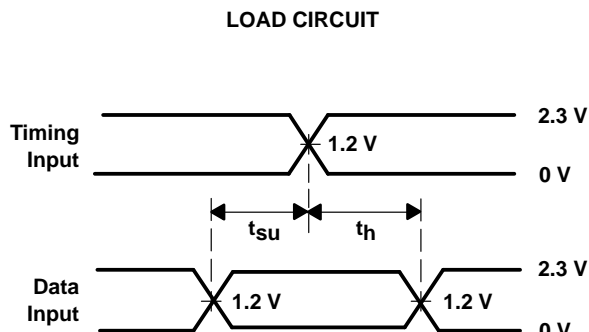
# PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

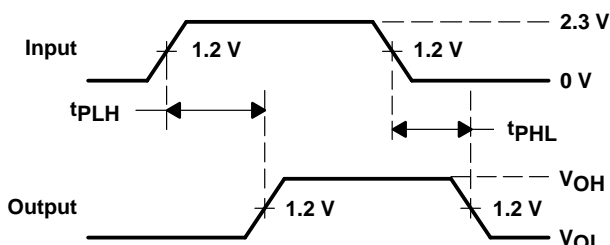


LOAD CIRCUIT

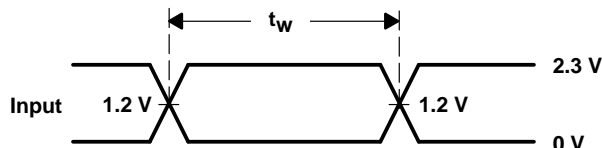
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	4.6 V
$t_{PHZ}/t_{PZH}$	GND



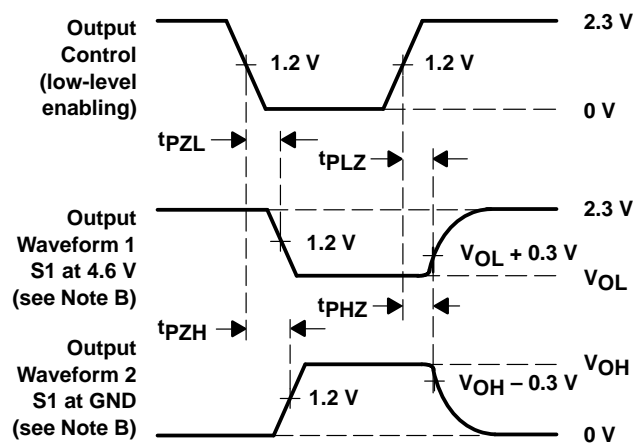
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

# SN74ALVCH162827

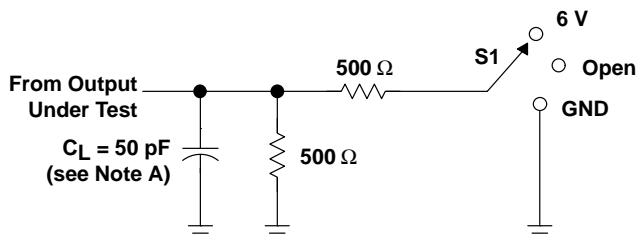
## 20-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

SCES013B – JULY 1995 – REVISED DECEMBER 1996

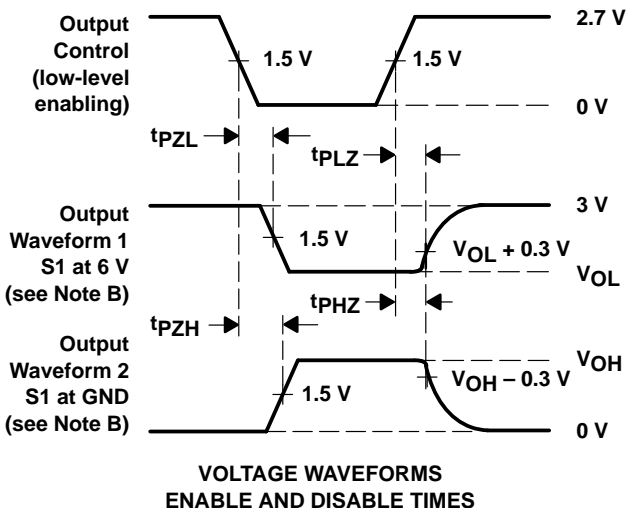
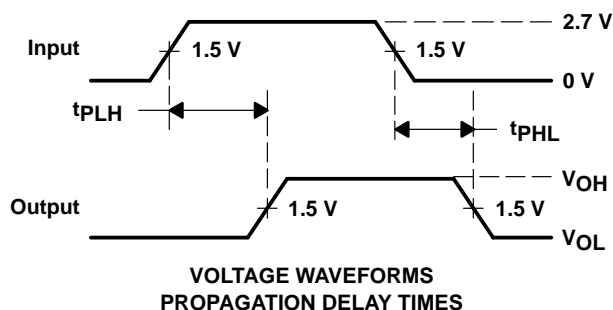
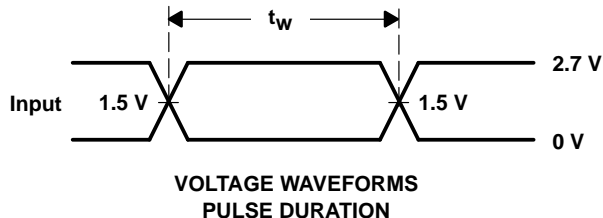
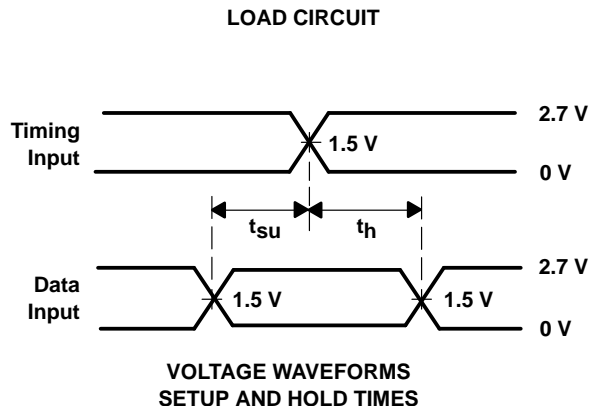
#### PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.