- *EPIC*™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Power Off Disables Inputs/Outputs, Permitting Live Insertion**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Package, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs**

SN54LVCH244A . . . J OR W PACKAGE
SN74LVCH244A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	20	V_{CC}
1A1	2	19	2$\overline{OE}$
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1

SN54LVCH244A . . . FK PACKAGE
(TOP VIEW)

Top pins: 2Y4, 1A1, 1$\overline{OE}$, V_{CC}, 2$\overline{OE}$ (pins 3, 2, 1, 20, 19)

1A2	4	18 1Y1
2Y3	5	17 2A4
1A3	6	16 1Y2
2Y2	7	15 2A3
1A4	8	14 1Y3

Bottom pins: 2Y1, GND, 2A1, 1Y4, 2A2 (pins 9, 10, 11, 12, 13)

description

These octal buffers/line drivers are designed for 2.7-V to 3.6-V V_{CC} operation.

The 'LVCH244A are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, these devices pass data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVCH244A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVCH244A is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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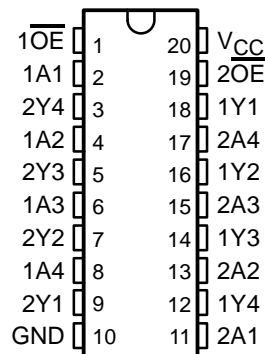
TEXAS INSTRUMENTS

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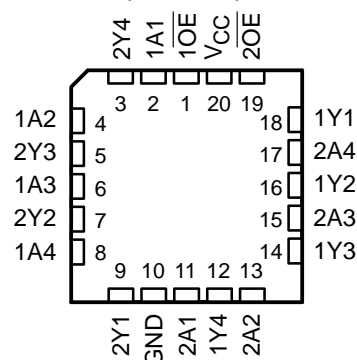# SN54LVCH244A, SN74LVCH244A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

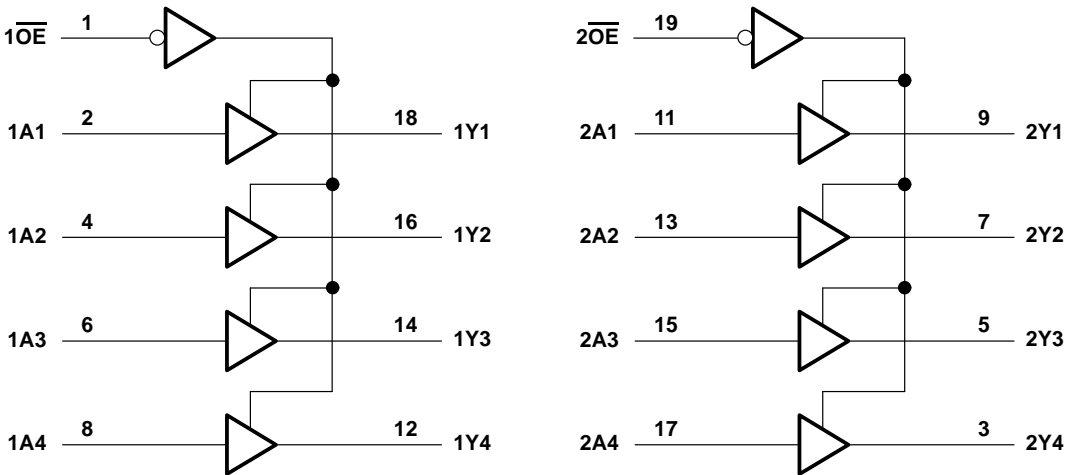SCES009D – JULY 1995 - REVISED JULY 1997

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†

1$\overline{OE}$ — 1 — EN

1A1 — 2 — ▷ ▽ — 18 — 1Y1
1A2 — 4 — — 16 — 1Y2
1A3 — 6 — — 14 — 1Y3
1A4 — 8 — — 12 — 1Y4

2$\overline{OE}$ — 19 — EN

2A1 — 11 — ▷ ▽ — 9 — 2Y1
2A2 — 13 — — 7 — 2Y2
2A3 — 15 — — 5 — 2Y3
2A4 — 17 — — 3 — 2Y4
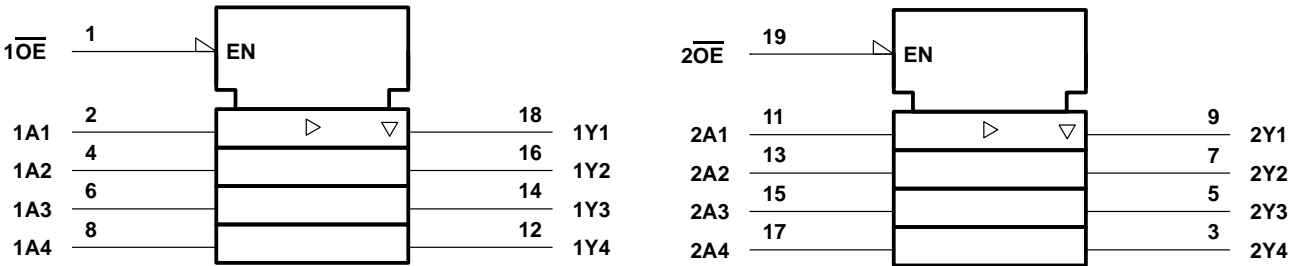
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

1$\overline{OE}$ — 1

1A1 — 2 — 18 — 1Y1

1A2 — 4 — 16 — 1Y2

1A3 — 6 — 14 — 1Y3

1A4 — 8 — 12 — 1Y4

2$\overline{OE}$ — 19

2A1 — 11 — 9 — 2Y1

2A2 — 13 — 7 — 2Y2

2A3 — 15 — 5 — 2Y3

2A4 — 17 — 3 — 2Y4

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INSTRUMENTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 6.5 V

Input voltage range, V_I (see Note 1) .... –0.5 V to 6.5 V

Voltage range applied to any output in the high-impedance or power-off state, V_O
   (see Note 1) .... –0.5 V to 6.5 V

Voltage range applied to any output in the high or low state, V_O
   (see Notes 1 and 2) .... –0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} ($V_I < 0$) .... –50 mA

Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±50 mA

Continuous output current, I_O ($V_O = 0$ to V_{CC}) (see Note 2) .... ±50 mA

Continuous current through V_{CC} or GND .... ±100 mA

Package thermal impedance, θ_{JA} (see Note 3): DB package .... 115°C/W
                                DW package .... 97°C/W
                                PW package .... 128°C/W

Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
        2. The value of V_{CC} is provided in the recommended operating conditions table.
        3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVCH244A		SN74LVCH244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	2	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3 state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12		–12	mA
		V_{CC} = 3 V		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12		12	mA
		V_{CC} = 3 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	0	10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

TEXAS
INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	SN54LVCH244A			SN74LVCH244A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	I_{OH} = −100 µA		2.7 V to 3.6 V	V_{CC}−0.2			V_{CC}−0.2			V
	I_{OH} = −12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I_{OH} = −24 mA		3 V	2.2			2.2			
V_{OL}	I_{OL} = 100 µA		2.7 V to 3.6 V			0.2			0.2	V
	I_{OL} = 12 mA		2.7 V			0.4			0.4	
	I_{OL} = 24 mA		3 V			0.55			0.55	
I_I	V_I = 0 to 5.5 V		3.6 V			±15			±5	µA
I_{off}	V_I or V_O = 5.5 V		0						±10	µA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75			75			µA
	V_I = 2 V			−75			−75			
	V_I = 0 to 3.6 V‡		3..6 V			±500			±500	
I_{OZ}	V_O = 0 to 5.5 V		3.6 V			±15			±10	µA
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			10			10	µA
	3.6 V ≤ V_I ≤ 5.5 V§					10			10	
ΔI_{CC}	One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500			500	µA
C_i	V_I = V_{CC} or GND		3.3 V		4	12		4		pF
C_O	V_O = V_{CC} or GND		3.3 V		5.5	12		5.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ This applies in the disabled state only.

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVCH244A				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1	6.5		7.5	ns
t_{en}	$\overline{OE}$	Y	1	8		9	ns
t_{dis}	$\overline{OE}$	Y	1	7		8	ns
$t_{sk(o)}$†				1.5			ns

† Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVCH244A				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.5	4.9		5.9	ns
t_{en}	$\overline{OE}$	Y	1	6.2		7.6	ns
t_{dis}	$\overline{OE}$	Y	1.5	6.5		7	ns
$t_{sk(o)}$†				1.5			ns

† Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	C_L = 0,	f = 10 MHz	47	pF
	Outputs disabled			2	

PARAMETER MEASUREMENT INFORMATION
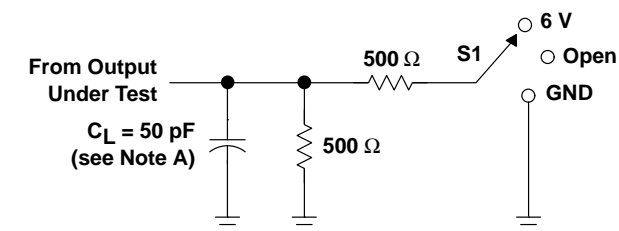
LOAD CIRCUIT

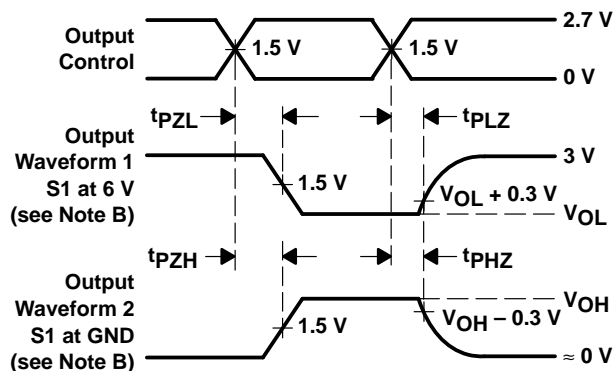| TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND
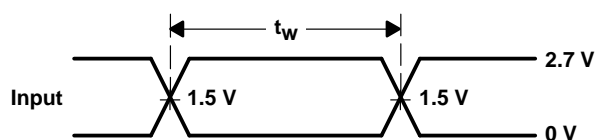
VOLTAGE WAVEFORMS
PULSE DURATION
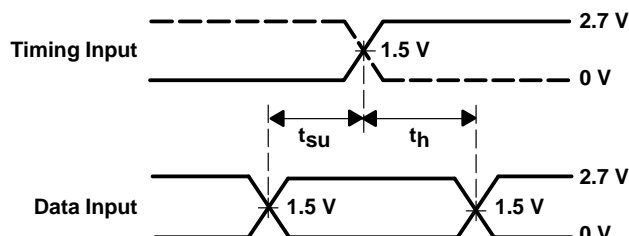
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
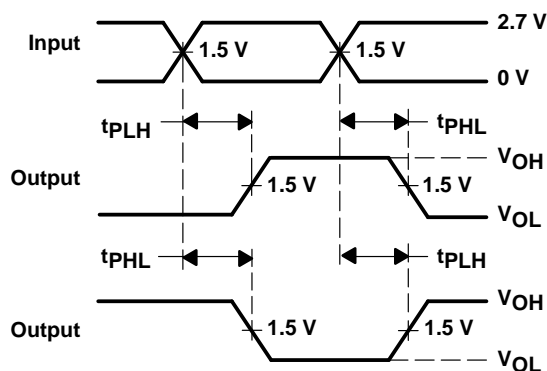
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
         Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
      D. The outputs are measured one at a time with one transition per measurement.
      E. t_{PZL} and t_{PZH} are the same as t_{en}.
      F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
      G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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