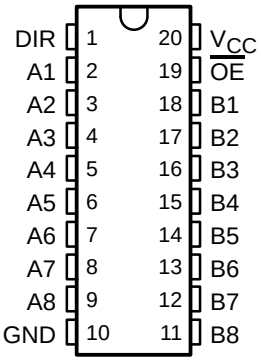
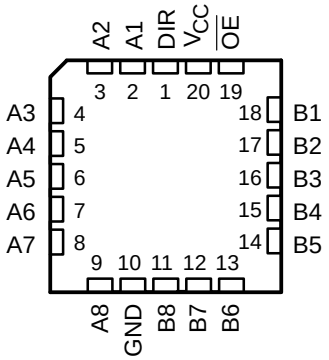
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Power Off Disables Inputs/Outputs, Permitting Live Insertion**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs**

SN54LVCH245A . . . J OR W PACKAGE
SN74LVCH245A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVCH245A . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for 2.7-V to 3.6-V V_{CC} operation.

The ’LVCH245A are designed for asynchronous communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

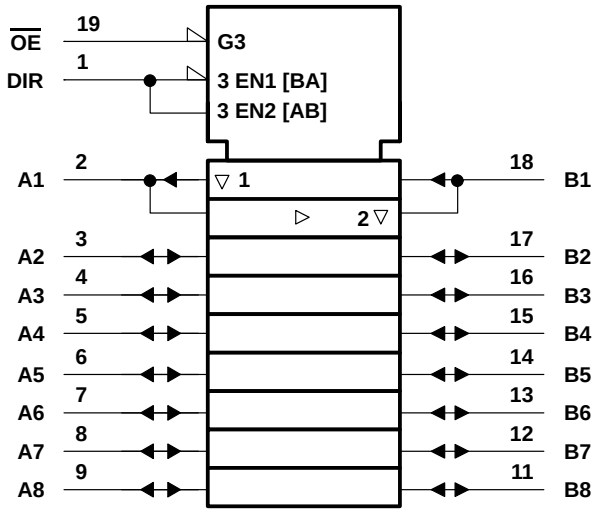
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVCH245A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVCH245A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

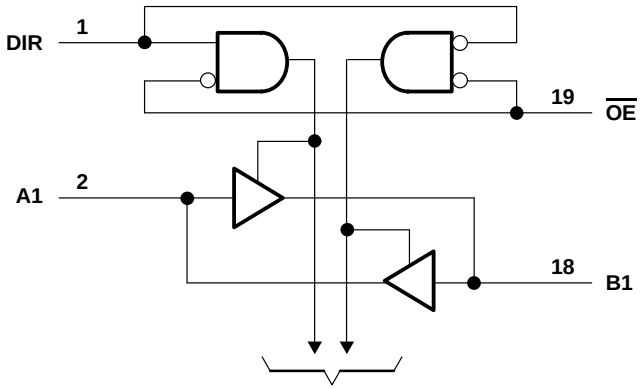
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 6.5 V
Input voltage range, V_I: Except I/O ports (see Note 1) . . . . . –0.5 V to 6.5 V
I/O ports (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) (see Note 2) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . . 115°C/W
DW package . . . . . 97°C/W
PW package . . . . . 128°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVCH245A		SN74LVCH245A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	2	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3 state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12		–12	mA
		V_{CC} = 3 V		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12		12	mA
		V_{CC} = 3 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	0	10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	SN54LVCH245A			SN74LVCH245A			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}		I_{OH} = –100 μA		2.7 V to 3.6 V	V_{CC}–0.2			V_{CC}–0.2			V
		I_{OH} = –12 mA		2.7 V	2.2			2.2			
				3 V	2.4			2.4			
		I_{OH} = –24 mA		3 V	2.2			2.2			
V_{OL}		I_{OL} = 100 μA		2.7 V to 3.6 V			0.2			0.2	V
		I_{OL} = 12 mA		2.7 V			0.4			0.4	
		I_{OL} = 24 mA		3 V			0.55			0.55	
I_I	Control inputs	V_I = 0 to 5.5 V		3.6 V			±15			±5	μA
I_{off}		V_I or V_O = 5.5 V		0						±10	μA
$I_{I(hold)}$		V_I = 0.8 V		3 V	75			75			μA
		V_I = 2 V			–75			–75			
		V_I = 0 to 3.6 V‡		3..6 V			±500			±500	
I_{OZ}§		V_O = 0 to 5.5 V		3.6 V			±15			±10	μA
I_{CC}		V_I = V_{CC} or GND	I_O = 0	3.6 V			10			10	μA
		3.6 V ≤ V_I ≤ 5.5 V¶					10			10	
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500			500	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		4	12		4		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		5.5	12		5.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.
¶ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVCH245A				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	1	7		8	ns
t_{en}	$\overline{OE}$	A or B	1	8.5		9.5	ns
t_{dis}	$\overline{OE}$	A or B	1	7.5		8.5	ns
$t_{sk(o)}$†				1			ns

† Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

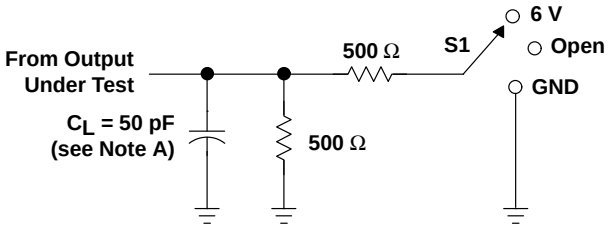
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVCH245A				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	1.5	6.3		7.3	ns
t_{en}	$\overline{OE}$	A or B	1.5	8.5		9.5	ns
t_{dis}	$\overline{OE}$	A or B	1.7	7.5		8.5	ns
$t_{sk(o)}$†				1			ns

† Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

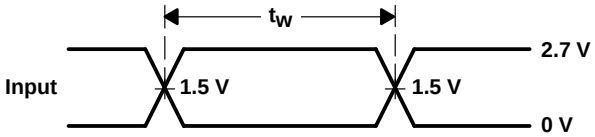
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 0, f = 10 MHz	47	pF
		Outputs disabled		2	

PARAMETER MEASUREMENT INFORMATION

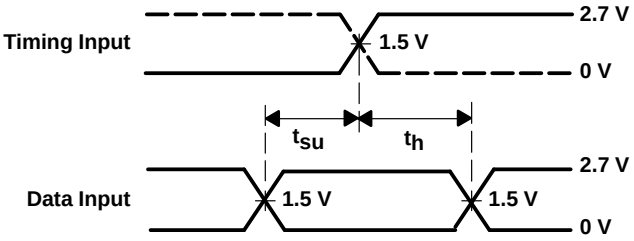


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

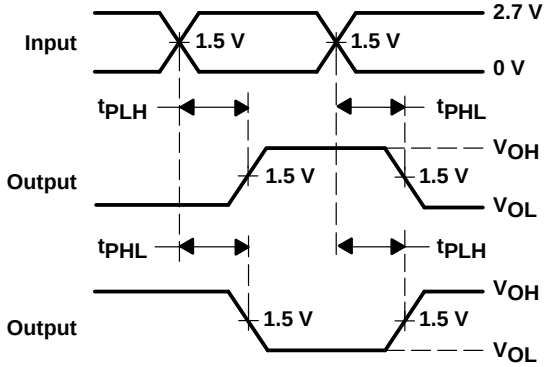
LOAD CIRCUIT



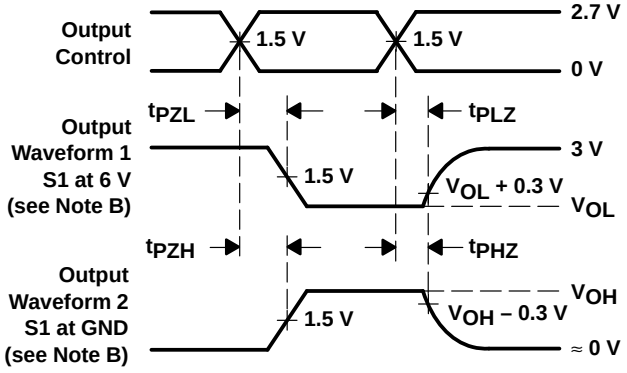
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PZL} and t_{PZH} are the same as t_{en}.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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