SN54LVT16601, SN74LVT16601
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCES002A – JULY 1994 – REVISED JULY 1995

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Support Live Insertion**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54LVT16601 . . . WD PACKAGE
SN74LVT16601 . . . DGG OR DL PACKAGE
(TOP VIEW)

Pin	Left		Right	Pin
1	$\overline{OEAB}$		CLKENAB	56
2	LEAB		CLKAB	55
3	A1		B1	54
4	GND		GND	53
5	A2		B2	52
6	A3		B3	51
7	V_{CC}		V_{CC}	50
8	A4		B4	49
9	A5		B5	48
10	A6		B6	47
11	GND		GND	46
12	A7		B7	45
13	A8		B8	44
14	A9		B9	43
15	A10		B10	42
16	A11		B11	41
17	A12		B12	40
18	GND		GND	39
19	A13		B13	38
20	A14		B14	37
21	A15		B15	36
22	V_{CC}		V_{CC}	35
23	A16		B16	34
24	A17		B17	33
25	GND		GND	32
26	A18		B18	31
27	$\overline{OEBA}$		$\overline{CLKBA}$	30
28	LEBA		CLKENBA	29

description

The 'LVT16601 are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

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description (continued)

Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{\text{CLKENAB}}$ and $\overline{\text{CLKENBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable $\overline{\text{OEAB}}$ is active low. When $\overline{\text{OEAB}}$ is low, the outputs are active. When $\overline{\text{OEAB}}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16601 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16601 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16601 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE[†]

INPUTS					OUTPUT
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0[‡]
H	L	L	X	X	B_0[‡]
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0[‡]
L	L	L	H	X	B_0[§]

[†] A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.
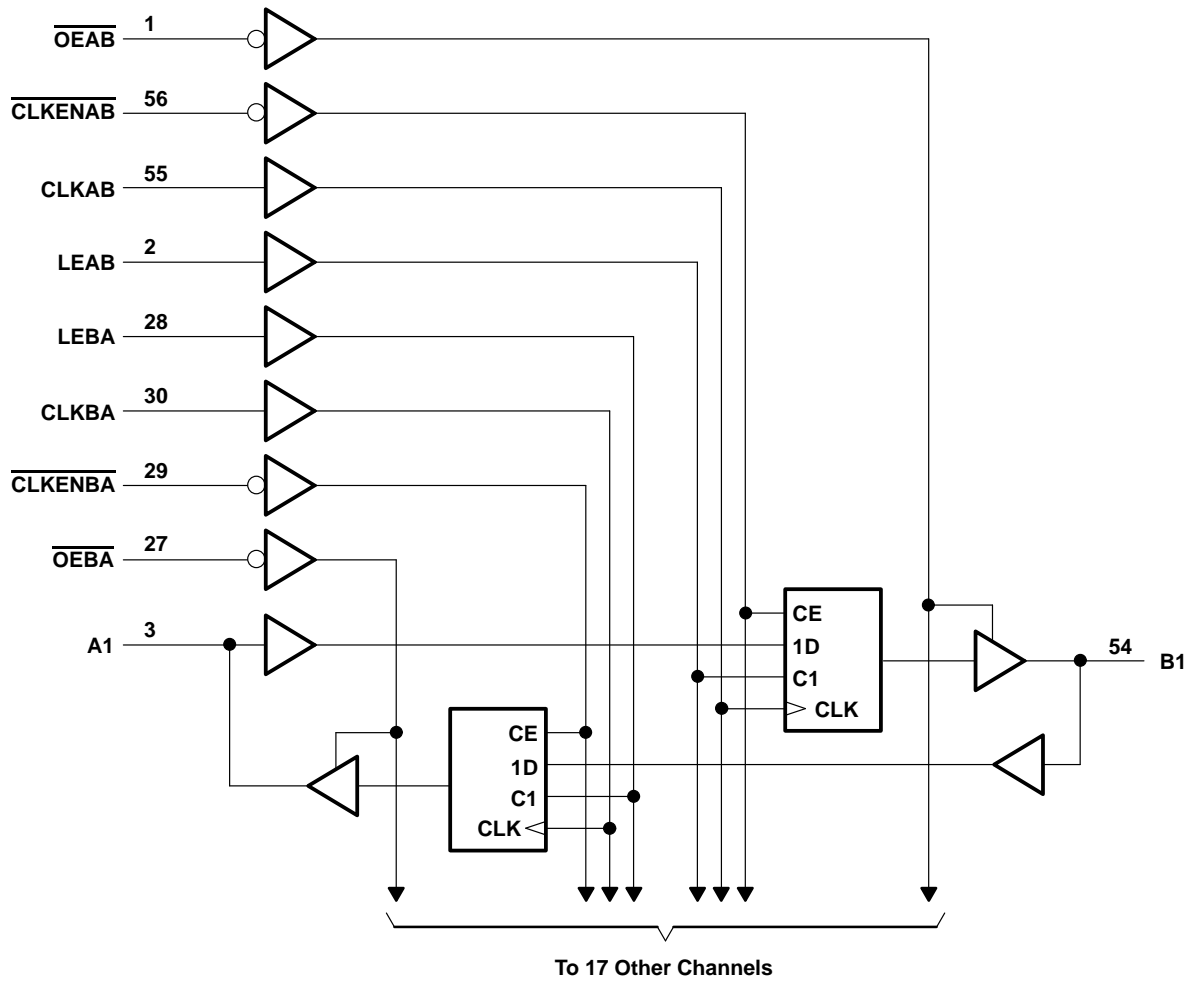
[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

logic diagram (positive logic)

To 17 Other Channels

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	−0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16601	96 mA
SN74LVT16601	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16601	48 mA
SN74LVT16601	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LVT16601		SN74LVT16601		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16601			SN74LVT16601			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 μA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 μA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control inputs			±1			±1	μA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				5			5	
		V_I = 0				−10			−10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	μA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			μA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	μA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	μA
I_{CC}	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND		Outputs high			0.12			0.12	mA
			Outputs low			5			5	
			Outputs disabled			0.12			0.12	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	V_I = 3 V or 0				3.5			3.5		pF
C_{io}	V_O = 3 V or 0				12			12		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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