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Application Report

GTL/BTL: A Low-Swing Solution for High-Speed Digital Logic

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TEXAS INSTRUMENTS

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Introduction

This application report examines the requirements for a low-swing interface in high-speed digital systems and how well this need is addressed by two interface standards: backplane transceiver logic (BTL) and Gunning transceiver logic (GTL). Both interface standards attempt to improve the performance of high-speed digital systems by reducing the difference between the logic high-voltage level and the logic low-voltage level.

A comparison of various performance criteria, such as power consumption, noise immunity, capacitive loading, speed, and packaging, shows that GTL and BTL provide a compelling solution in both point-to-point and backplane environments. Guidelines for system designs using Texas Instruments (TI) GTL and BTL products are addressed, including associated voltage supplies and proper termination techniques.

Test Setup

The TI GTL16612 and FB1650 were used to study the various performance levels. A backplane-like design has been established to perform the laboratory work supporting this application report. Four boards with 2-in. stubs and 50-Ω interconnecting transmission lines were used to simulate the backplane environment. A 50-MHz frequency was used unless otherwise noted. The output supply voltage (V_{TT}) was supplied through a resistor at each end of the backplane (50-Ω to 1.2 V for GTL and 33-Ω to 2.1 V for BTL) for both families as specified in both IEEE (BTL) and JEDEC (GTL) standards. Figure 1 shows the backplane model with all four boards connected.

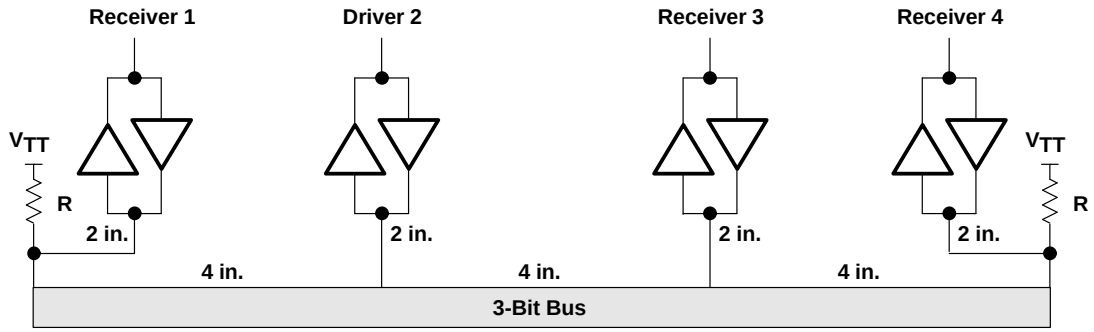

Figure 1. Backplane Model With All Four Boards Connected

Another design has been used to simulate the transmission-environment effect when transferring data across a longer point-to-point transmission line. Figure 2 shows the same backplane model with only one driver and one receiver used to transfer the data across 12-in., 28-in., and 48-in. transmission lines.

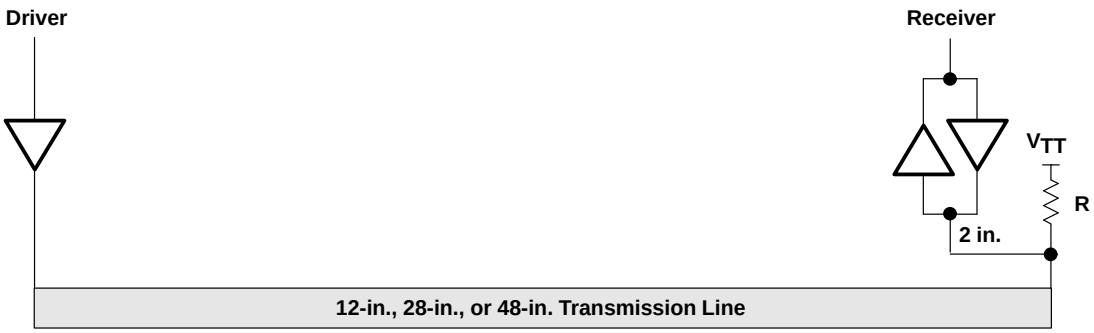

Figure 2. Point-to-Point Model With Only One Driver and One Receiver Connected

Advantages of GTL or BTL Over CMOS/TTL

BTL and GTL were developed to solve the bus-driving problem associated with TTL and to enhance the performance of point-to-point and backplane applications. BTL and GTL also eliminate the need for the extra time required for the TTL signal to settle due to reflection and noise generated when switching. The 1-V swing of both signals versus the 3-V to 5-V swing of TTL and CMOS signals helps reduce the noise generated on the bus when the outputs are switching simultaneously. Table 1 shows the minimum high-level output voltage (V_{OH}) and the maximum low-level output voltage (V_{OL}) of CMOS, TTL, BTL, and GTL signals.

Table 1. V_{OH} and V_{OL} Levels for Various Families

LOGIC LEVEL	V_{OH}min (V)	V_{OL}max (V)
CMOS	3.8	0.44
TTL	2.4	0.55
BTL	2.1	1
GTL	1.2	0.4

BTL and GTL buffers are designed with minimal output capacitance (5 pF maximum) compared to a TTL output buffer (8 pF to 15 pF typical). A TTL or CMOS output capacitance, coupled with the capacitance of the connectors, traces, and vias reduces the characteristic impedance of the backplane. For high-frequency operation, this phenomenon makes it difficult for the TTL or CMOS driver to switch the signal on the incident wave. A TTL or CMOS device needs a higher drive current than presently available to be able to switch the signal under these conditions. However, increasing the output drive clearly increases the output capacitance. This scenario again reduces the characteristic impedance even more. That is why a lower signal-swing family with reduced output capacitance, such as BTL or GTL, is recommended when designing high-speed backplanes.

GTL Family Input and Output Structure

The GTL input receiver is a differential comparator with one side connected to the externally provided reference voltage, V_{REF} (0.8 V typical). The threshold is designed with a precise window for maximum noise immunity ($V_{IH} = V_{REF} + 50$ mV and $V_{IL} = V_{REF} - 50$ mV). The output driver is an open-drain n-channel device which, when turned off, is pulled up to the output supply voltage ($V_{TT} = 1.2$ V typical). When turned on, the device can sink up to 40 mA of current (I_{OL}) at a maximum output voltage (V_{OL}) of 0.4 V. The output is designed for a 50-Ω transmission line terminated at both ends (25-Ω total load). The inputs and outputs are designed to work independently of the device's V_{CC}. They can communicate with devices designed for 5-V, 3.3-V, or even 2.5-V V_{CC}. The TTL input is a 5-V tolerant 3.3-V CMOS inverter that can interface with 5-V TTL signals. Bus hold is also provided on the TTL port to eliminate the need for external resistors when the inputs and outputs are unused or floating. The TTL output is a bipolar output. It is similar to the LVT output structure.[1] At this time, devices require two power supplies to function: a 5-V supply [$V_{CC(5)}$] for the GTL and a 3.3-V supply [$V_{CC(3.3)}$] for the LVTTL. The 5-V supply is used only on the GTL16612 and GTL16616. The maximum operating frequency of the family is 95 MHz (GTL16612 and GTL16616). The future-generation family, which will be available in mid-1996, will operate up to 200 MHz in both directions (GTL to TTL or TTL to GTL) and will have a single 3.3-V power supply.[1] Figure 3 shows a typical GTL input and output circuit.

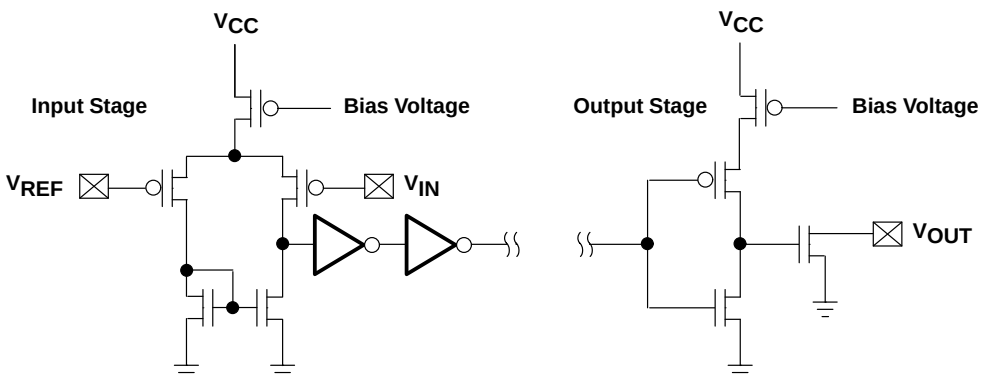

Figure 3. Typical GTL Input and Output Cells

BTL Family Input and Output Structure

The BTL input receiver is a differential amplifier with one side connected to an internal reference voltage. The threshold is designed with a narrow window (V_{IH} = 1.62 V and V_{IL} = 1.47 V). Unlike GTL, BTL requires a separate supply voltage for the threshold circuit to eliminate any noise generated by the switching outputs. The output driver is an open-collector output with a termination resistor selected to match the bus impedance. When the device is turned off, the output is pulled up to the output supply voltage (V_{TT} = 2.1 V typical). The inputs and outputs work independently of the device's V_{CC}. They can communicate with devices designed for 5-V or 3.3-V V_{CC}. The TTL input is a 5-V CMOS inverter, and the output is a bipolar output similar to the ABT output structure.[1] BTL requires three power supplies: the main power supply (V_{CC}), the bias generator supply (BG V_{CC}), and the bias supply voltage (BIAS V_{CC}) that establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected. The maximum operating frequency of the BTL family is 75 MHz, depending on the application as well as the board layout. Figure 4 shows a typical BTL input and output circuit.

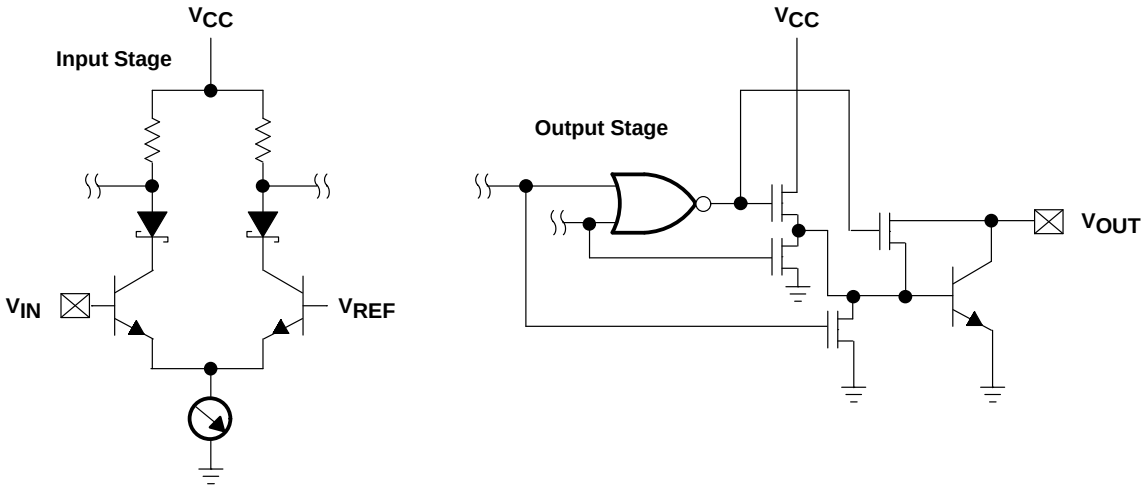

Figure 4. Typical BTL Input and Output Cells

Power Consumption

Several factors influence the power consumption of a device: frequency of operation, number of outputs switching, load capacitance, number of TTL-level inputs, junction temperature, ambient temperature, and thermal resistance of the device. For BTL and GTL devices, the output power is supplied externally by the output voltage supply (V_{TT}). The maximum operating frequency is limited by the thermal characteristics of the package. TI provides package power-dissipation information in data sheets under "absolute maximum ratings". These values are calculated using a junction temperature of 150°C and a board trace length of 750 mils (no airflow).[3] Traces, power planes, connectors, and cooling fans play an important role in improving heat dissipation. Figure 5 shows the power consumption of BTL and GTL devices driving the backplane described above. As the frequency increases, GTL16612 power consumption does not increase as fast as the FB1650. This characteristic is due to the predominant use of CMOS technology, the lower drive current, and the lower voltage swing of GTL (0.8-V swing for GTL versus 1-V swing for BTL). Lower drive current and lower voltage swing are two of the benefits that GTL provides over BTL drivers. A power-consumption comparison (see Table 2) illustrates the advantage of GTL over BTL when 160 active inputs and outputs are switching.[2] Another benefit GTL offers is that the family uses the common 56-pin SSOP and TSSOP packages rather than the 100-pin thin quad flat package (TQFP) with a heat slug mounted above the die in BTL parts. The pin count on the TQFP package is almost twice the pin count of the SSOP or TSSOP packages.

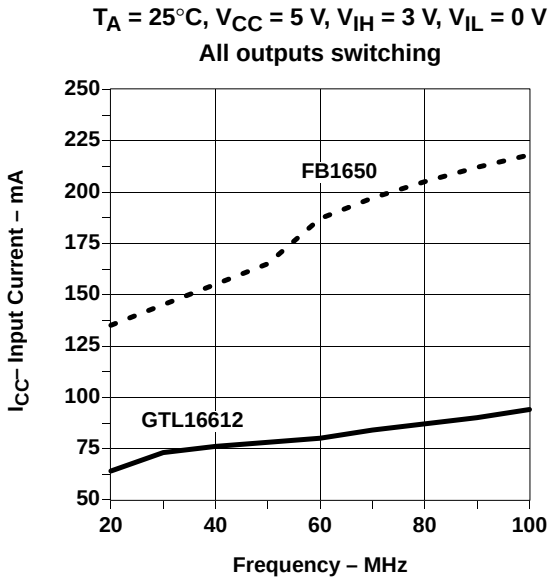

Figure 5. FB1650 and GTL16612 Power Consumption With All Outputs Switching

Table 2. Power Comparison (160 Active Inputs and Outputs)

TECHNOLOGY	POWER (W)	TERMINATION (BOTH ENDS)
BTL	11	33 Ω to 2.1 V
GTL	2	50 Ω to 1.2 V

Simultaneous Switching

In a given digital circuit, there is a large change in current over a very short time when multiple outputs switch simultaneously. As this increased current flows through the bond wires and the leadframe, it develops a voltage across the wire's inductance. This feedback mechanism is known as simultaneous switching noise (SSN). This noise manifests itself as V_{OL} or V_{OH} voltage bounce at the package pin(s).

From basic circuit analysis, the induced voltage across an inductor is defined as:

$$v = L\frac{di}{dt} \quad \textbf{(1)}$$

Where:

L = Inductance
di/dt = Rate of change of the current

The current through an output is dependent on the voltage level and the load at the output, which can be expressed mathematically as:

$$i = C\frac{dv_{out}}{dt} \quad \textbf{(2)}$$

Analysis of equations (1) and (2) clearly shows that because of the lower voltage swing, GTL and BTL offer better noise immunity compared to TTL or CMOS outputs.

As the speed of today's circuits increases, the current rate of change (di/dt) increases and so does the susceptibility to SSN, i.e., voltage bounce (GND and V_{CC}). The standard methodology devised by the industry to measure voltage bounce is to keep one output at either logic high (V_{OH}) or logic low (V_{OL}) and to switch all other outputs at a predefined frequency. Figures 6 through 9 compare both GTL and BTL for noise immunity as 17 outputs are switching simultaneously.

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω

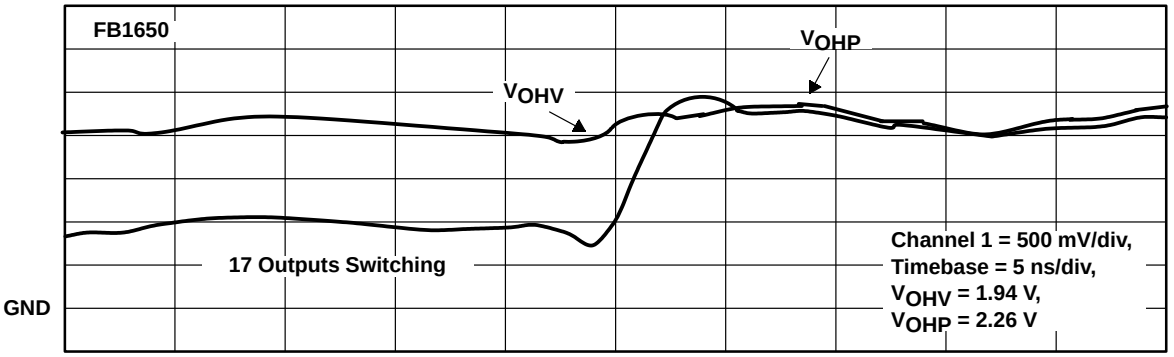

Figure 6. FB1650 High Output Voltage Peak and Valley Noise on an Unswitched Output

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω

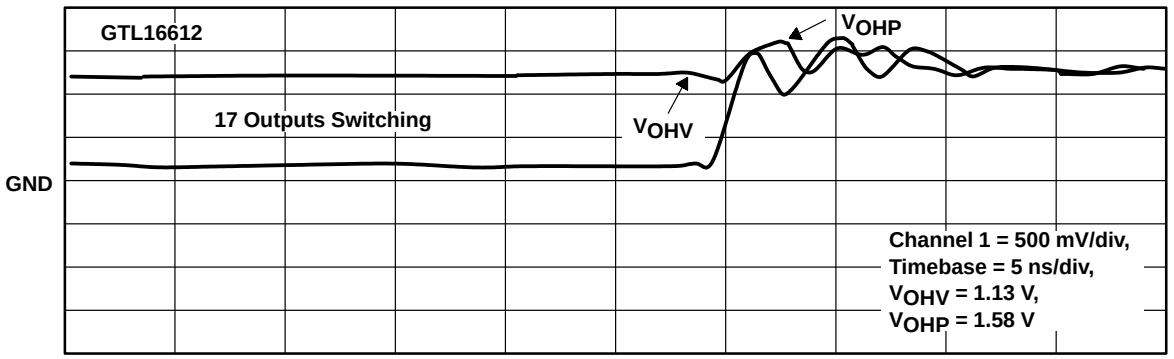

Figure 7. GTL16612 High Output Voltage Peak and Valley Noise on an Unswitched Output

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω

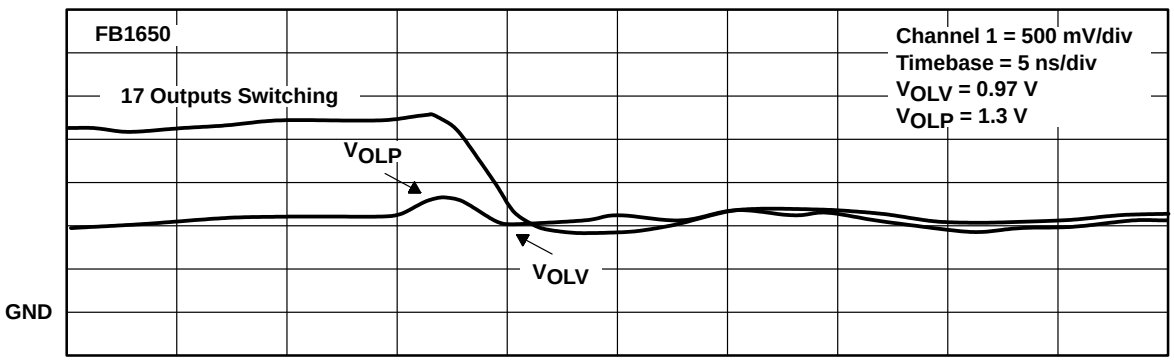

Figure 8. FB1650 Low Output Voltage Peak and Valley Noise on an Unswitched Output

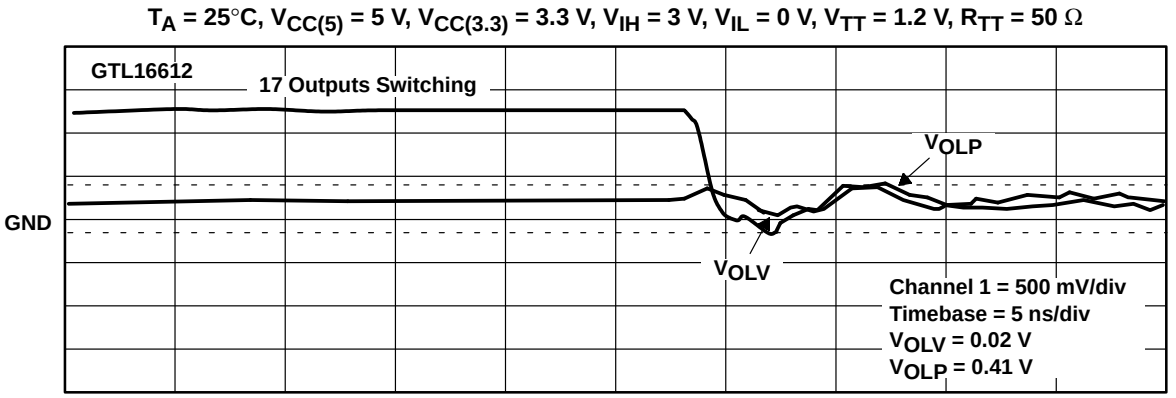

Figure 9. GTL16612 Low Output Voltage Peak and Valley Noise on an Unswitched Output

Output Capacitance

GTL and BTL devices are designed to meet a 5-pF capacitance on their input and output ports (B port). Figure 10 shows the variation of the output capacitance across both processes.

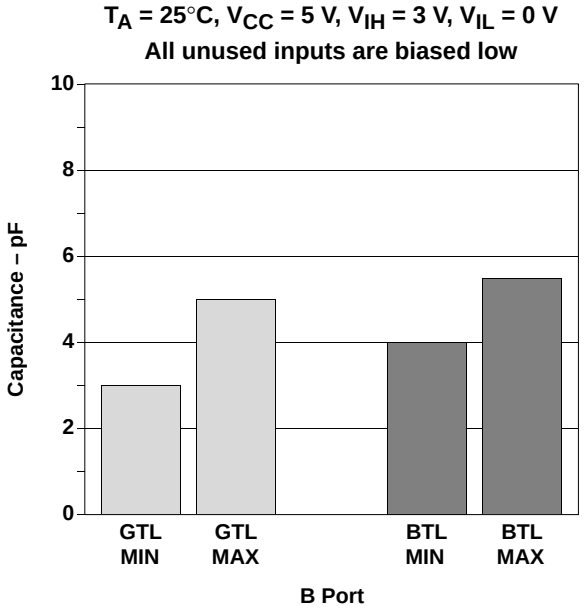

Figure 10. Capacitance Variation Across Process

Slew Rate

Slew rate plays an important role in backplane or point-to-point application designs. The slower the output slew rate of a device, the less susceptible the signal is to reflections and noise. Using the backplane model (see Figures 1 and 2), the output slew rate (t_r and t_f) of the driving device was taken under the following conditions: a 10-in., 50-Ω transmission line and a single termination to V_{TT} at the receiver end. Figures 11 through 14 show the rise and fall times of both devices taken between the two specified voltages of 0.5 V to 1 V for GTL and 1.3 V to 1.8 V for BTL. Both the BTL and GTL slew rates are acceptable.

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω, Frequency = 10 MHz

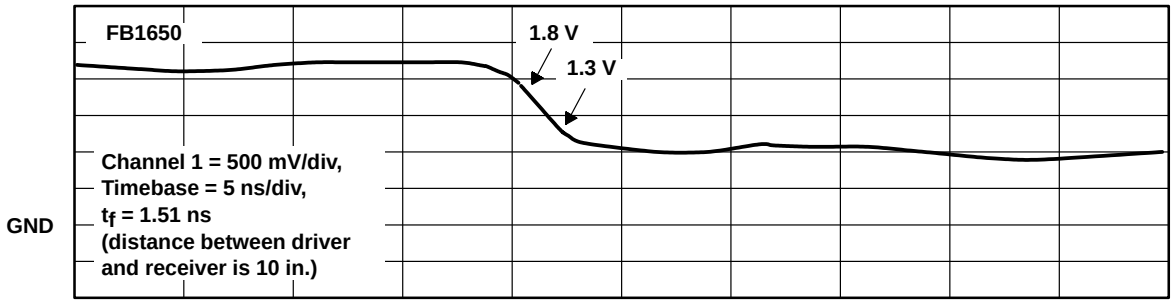

Figure 11. FB1650 Fall Time Measured Between 1.3 V and 1.8 V

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω, Frequency = 10 MHz

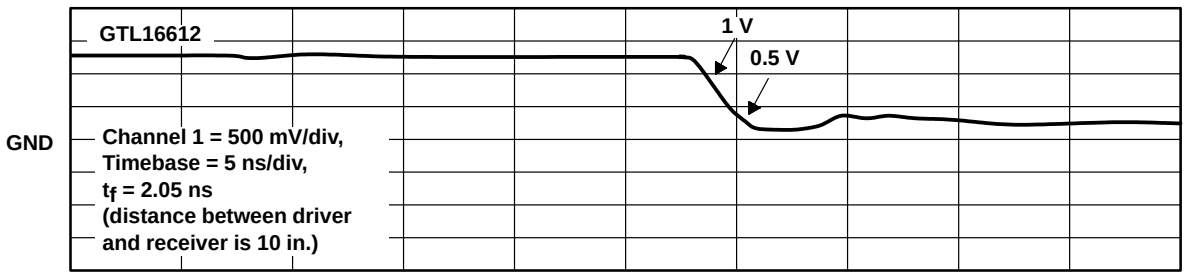

Figure 12. GTL16612 Fall Time Measured Between 0.5 V and 1 V

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω, Frequency = 10 MHz

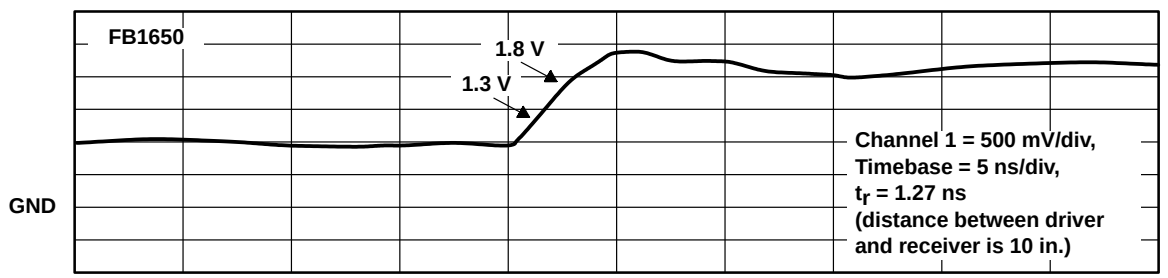

Figure 13. FB1650 Rise Time Measured Between 1.3 V and 1.8 V

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω, Frequency = 10 MHz

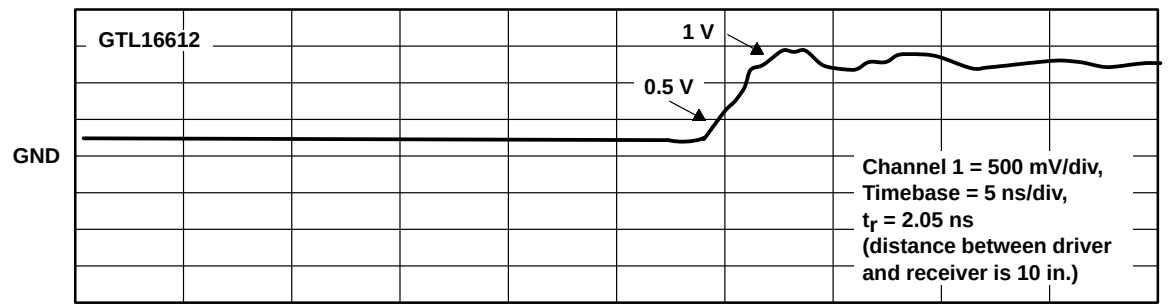

Figure 14. GTL16612 Rise Time Measured Between 0.5 V and 1 V

Signal Integrity

Figures 15 and 16 show the signal integrity of data propagating across the 50-Ω transmission line using three cable lengths (A = 12 in., B = 28 in., and C = 46 in.). The clock frequency is 75 MHz. The measurement was taken at the receiver end of the cable. The GTL output waveform has kept its input square-wave shape better than the BTL waveform has. The cable and the termination resistors used in this laboratory are not precisely matched; that is why a small reflection can be seen on the GTL outputs when switching low to high. In real systems, where both the termination resistor and the traces are matched, these reflections will be reduced.

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω, Frequency = 75 MHz

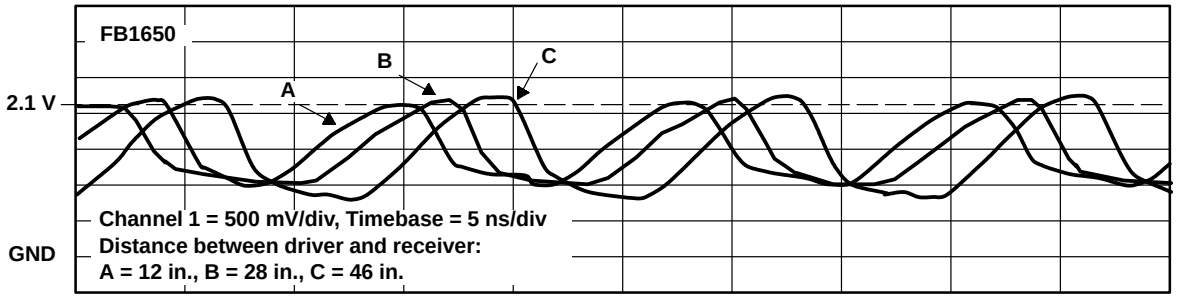

Figure 15. FB1650 Signal Integrity at the Receiver Input Using Different-Length Cables

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω, Frequency = 75 MHz

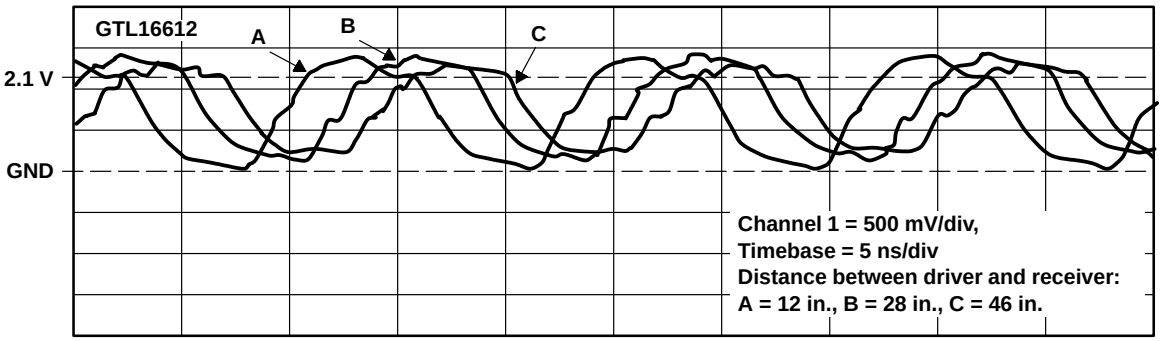

Figure 16. GTL16612 Signal Integrity at the Receiver Input Using Different-Length Cables

Design Considerations

To successfully design with the GTL family, several rules and techniques with regard to voltage generation and proper termination must be followed. First, both 3.3-V and 5-V V_{CC} are needed in the present generation of GTL devices (only the 3.3-V V_{CC} will be needed in the next-generation GTL). Second, the termination voltage (V_{TT} = 1.2 V) should be regulated from the 5-V V_{CC}, keeping in mind the current requirements of the outputs (40 mA per output). There are several linear regulators that are capable of performing this function. Depending on the design, the regulator could be either on the backplane itself or on the individual cards. Third, the reference voltage (V_{REF} = 0.8 V) must be generated from V_{TT}. The V_{REF} voltage can be generated using a simple voltage-divider circuit with an appropriate bypass capacitor (0.01 μF or 0.1 μF) placed as close as possible to the V_{REF} pin. The V_{REF} input circuitry consumes very little power (1 μA maximum). This enables several devices to have their V_{REF} pin connected to the same voltage-divider circuit, thus eliminating the need for multiple voltage-divider circuits (see Figure 17).

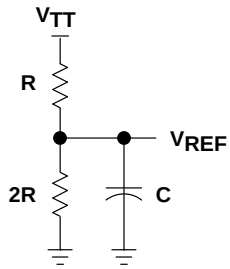

Figure 17. Proposed Circuit to Generate V_{REF}

For the BTL family, four power supplies and two grounds are connected. For live-insertion applications, the power-up sequence should be: the GND pin should make contact first, followed by BIAS V_{CC}. This sequence will precharge the board and the device capacitance and will establish a voltage between 1.62 V and 2.1 V on the BTL outputs. Next, the V_{CC} pin makes contact and, as V_{CC} ramps up, the BIAS V_{CC} circuitry starts to turn off. When V_{CC} reaches its final value, the BIAS V_{CC} circuitry is completely isolated and does not interfere with the device functionality. BG V_{CC} and BG GND pins supply power to the bias generator input circuitry. BG V_{CC} and BG GND must be isolated from the other power supplies to ensure signal integrity at the BTL input. The 2.1-V V_{TT} should be regulated from a higher voltage and should supply enough current to switch all 18 outputs (100 mA per output). V_{TT} variation should not exceed ±2% and it is recommended that proper bypass capacitors (0.01 μF or 0.1 μF) be used. The termination resistor should not exceed ±1% of its resistance value.

Table 3 gives the designer an estimate of the maximum number of loads allowed when designing with GTL and BTL families.[4] Note that crosstalk and poor board layout can degrade the overall quality of the backplane, thereby affecting the number of loads.

Using the formula:

$$t_r,\ t_f = 2.2 \times Z_S \times [(L \times C_O) + (N \times C_N)] \quad \textbf{(3)}$$

and assuming $t_r,\ t_f = t_p = \frac{1}{2f}$ (for worst case condition), the maximum number of loads on the backplane (N) can be calculated as follows:

$$N = \frac{1}{4.4 \times f \times Z_S \times C_N \times 10^{-6}} - \frac{L \times C_O}{C_N} \quad \textbf{(4)}$$

Where:

- t_r = Rise time of the device (ns)
- t_f = Fall time of the device (ns)
- Z_S = Output impedance of the source (Ω), 25 Ω for GTL, 16.5 Ω for BTL
- C_O = Characteristic capacitance per unit length of the transmission line (pF/in.) (see Table 3)
- L = Length of the backplane (in.)
- N = Maximum number of loads on the backplane
- C_N = Capacitance for each load (pF), 5 pF for the device, 5 pF for the connector
- t_p = Pulse width of the signal (ns)
- f = Frequency of the signal on the backplane (MHz)

Table 3. Typical Strip-Line Characteristics†

DIMENSIONS (mils)			LINE IMPEDANCE Z_O (Ω)	CAPACITANCE C_O (pF/in.)	t_{pd} (ns/in.)	MAXIMUM NUMBER OF LOADS		
						GTL		BTL
T	H	W				L = 12 in.	L = 16 in.	L = 24 in.
1.5	6	20	27	6.67	0.18	10	8	12
1.5	6	15	32	5.83	0.186	11	9	14
1.5	10	20	34	5.58	0.189	11	9	14
1.5	12	20	37	4.75	0.176	12	11	16
1.5	10	15	40	4.67	0.187	13	11	16
1.5	12	15	43	4	0.172	13	12	18
1.5	20	20	44	4	0.176	13	12	18
1.5	20	15	51	3.5	0.179	14	13	19
1.5	30	20	55	3.25	0.179	14	13	20
1.5	30	15	61	2.92	0.178	15	14	21

† The characteristic impedance of the strip line is based on the following:
er = 5, relative dielectric constant of the board material (G10 glass epoxy)
H = thickness of the insulation dielectric
T = cross-sectional length of the strip line
W = cross-sectional width of the strip line
Frequency of the signal on the backplane is 50 MHz.

Summary

Today's high-speed backplane and point-to-point applications require devices that can provide high performance, excellent signal integrity, and cost effectiveness. GTL and BTL transceivers are designed to meet these characteristics. Both transceiver families show similar skew, slew rate, and SSN performance. BTL is generally used for heavily loaded backplanes (100-mA I_{OL}) and for frequencies less than 75 MHz. However, the laboratory data presented in this report show that GTL is more suitable for designs that require high performance (up to 100 MHz for the present family and 200 MHz for the future generation) and low power consumption at low cost and minimum board space.

References

[1]Texas Instruments Incorporated, *ABT Advanced BiCMOS Technology Data Book*, 1994, literature number SCBD002B.

[2]Gunning, Bill; Yuan, Leo; Nguyen, Trung; Wong, Tony, *GTL: A Low-Voltage Swing Transmission Line Transceiver*, March 15, 1991.

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[4]Texas Instruments Incorporated, *Advanced Schottky Load Management*, 1987, literature number SDAA006.