Low-Voltage CMOS (LVC) Characterization Information

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TEXAS INSTRUMENTS

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Introduction

This application report provides Texas Instruments (TI) low-voltage CMOS (LVC) logic family characterization information to supplement data in the *Low-Voltage Logic Data Book* (literature number SCBD003B). This additional information is intended to help design engineers more accurately design their digital logic systems.

Although this application report focuses on the characteristics specific to TI's LVC logic family of devices, three other low-voltage logic (LVL) families exist. They are: low-voltage (LV), advanced low-voltage CMOS (ALVC), and low-voltage technology (LVT). Graphs and tables are provided to compare various devices. Unless otherwise noted, the data provided is typical data and should not be used as a minimum or maximum specification.

The main topics discussed are:

- The case for low voltage
- Considerations for interfacing to 5-V logic
- AC performance
- Power considerations
- Input characteristics
- Output characteristics
- Signal integrity
- LVC comparison to other LVL families
- SPICE models
- Advanced packaging
- Frequently asked questions

Appendixes A, B, and C provide characterization data on the SN74LVCH244, SN74LVC374A, and SN74LVC16245A.

For more information on TI's LVC logic products, please contact your local TI field sales office or an authorized distributor, or call TI at 1-800-336-5236.

The Case for Low Voltage

LVL, in the context of this application report, refers to devices designed specifically to operate from a 3.3-V power supply. Initially, an alternative method of achieving low-voltage operation was to use a device designed for 5-V operation, but power it with a 3.3-V supply. Although this resulted in 3.3-V characteristics, this method had significantly slower propagation time. Subsequently, parts were designed to operate using a 3.3-V power supply. This application report describes these devices.

A primary benefit of using a 3.3-V power supply as opposed to the traditional 5-V power supply is the reduced power consumption. Because power consumption is a function of the load capacitance, the frequency of operation, and the supply voltage, a reduction in any one of these is beneficial. Supply voltage has a square relationship in the reduction of power consumed, whereas load capacitance and frequency of operation have a linear effect. As a result, a small decrease in the supply voltage yields an exponential reduction in the power consumption. Equation 1 provides the dynamic component of the power calculation. (The calculation for computing the total power consumed is provided in the *Power Considerations* section of this application report.)

$$P_D(\text{dynamic}) = [\ (C_{pd} + C_L) \times V_{CC}{}^2 \times f\ ]N_{SW} \quad \textbf{(1)}$$

Where: C_{pd} = Power dissipation capacitance (F)
C_L = External load capacitance (F)
V_{CC} = Supply voltage (V)
f = Operating frequency (Hz)
N_{SW} = Total number of outputs switching

A reduction of power consumption provides several other benefits. Less heat is generated, which reduces problems associated with high temperature. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower temperature stress gradients on the device, and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. An additional benefit of the reduced power consumption is the extended life of the battery when a system is not powered by a regulated power supply.

Although a complete migration may not be feasible for a particular application, beginning to integrate 3.3-V components in a system still has benefits. If system parts are designed using 3.3-V parts, then when the remaining parts become available, converting the system completely to 3.3-V parts is a much smaller task. For example, having the internal parts of a personal computer powered from a 3.3-V power supply while having the memory powered from a 5-V power supply is a fairly common current configuration. Although LVL devices are not used throughout the entire design, this system is easily adapted to a complete 3.3-V system when 3.3-V memory becomes cost-effective.

Considerations for Interfacing to 5-V Logic

Interfacing 3.3-V devices to 5-V devices requires consideration of the logic switching levels of the driver and the receiver. Figure 1 illustrates the various switching standards for 5-V CMOS, 5-V TTL, and 3.3-V LVC. The switching levels for the 5-V TTL and the 3.3-V LVC are identical, whereas the 5-V CMOS switching levels are different. The impact of this must be considered when interfacing 3.3-V systems with 5-V systems.

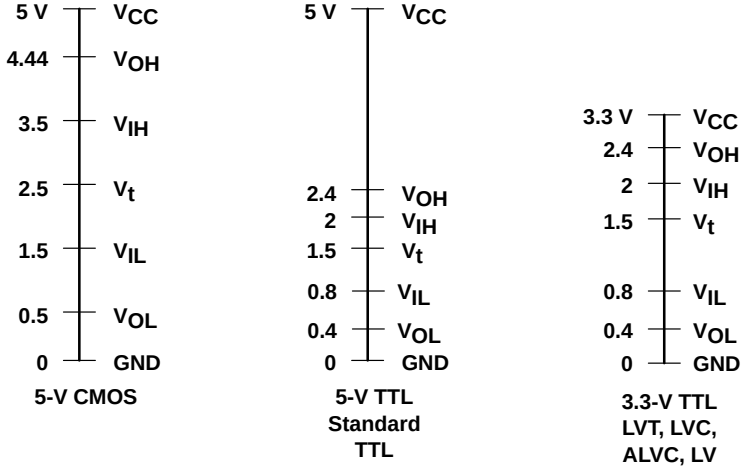


Figure 1. Comparison of 5-V CMOS, 5-V TTL, and 3.3-V LVC Switching Standards

Depending on the specific parts used in a system, four different cases can result. These cases are illustrated in Figure 2.

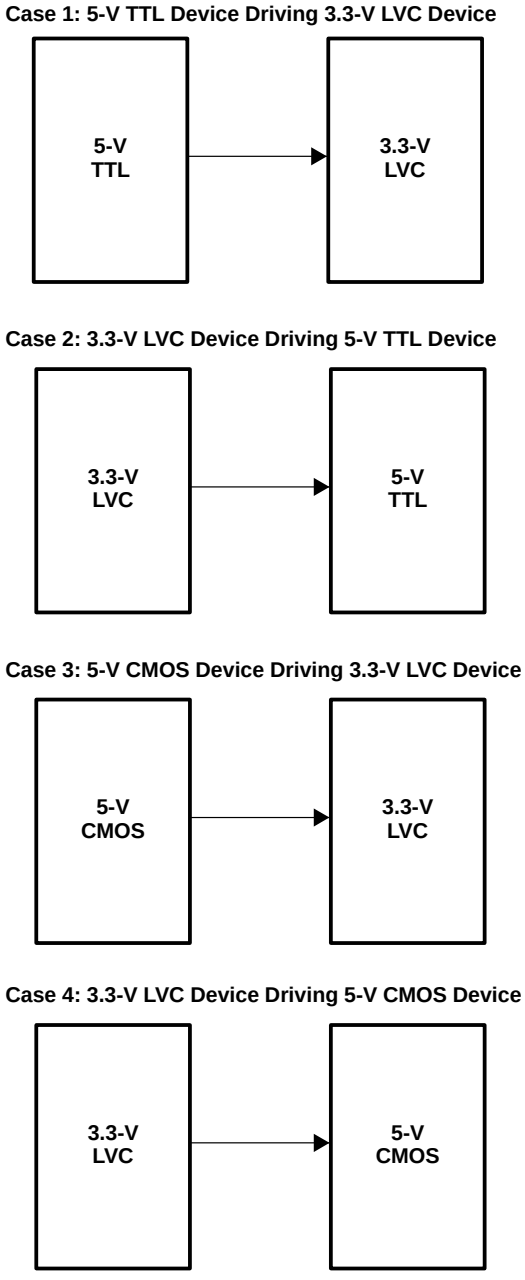


Figure 2. Summary of Four Cases When Interfacing 3.3-V Devices With 5-V Devices

Case 1 addresses a 5-V TTL device driving a 3.3-V LVC device. As shown in Figure 1, the switching levels for 5-V TTL and 3.3-V LVC are the same. Since LVC 5-V tolerant devices can withstand a dc input of 6.5 V, interfacing these two devices does not require additional components or further design efforts.

TI's crossbar technology (CBT) switches can be used to translate from 5-V TTL to 3.3-V LVC. This is accomplished by using an external diode to create a 0.7-V drop (reducing 5 V to 4.3 V) with the CBT (of which the Field Effect Transistor has a gate-to-source voltage drop of 1 V) that results in a net 3.3-V level. TI produces a CBTD device that incorporates the diode as part of the chip, thereby eliminating the need for an external diode.

Case 2 occurs when a 3.3-V LVC device drives a 5-V TTL device. The switching levels are the same and it is possible to interface under this configuration without additional circuitry or devices. Driving a 5-V device from a 3.3-V device without additional complications or circuitry may seem odd, but as long as the 3.3-V device produces V_{OH} and V_{OL} levels of 2.4 V and 0.4 V, the input of the 5-V device reads them as valid levels since V_{IH} and V_{IL} are 2 V and 0.8 V.

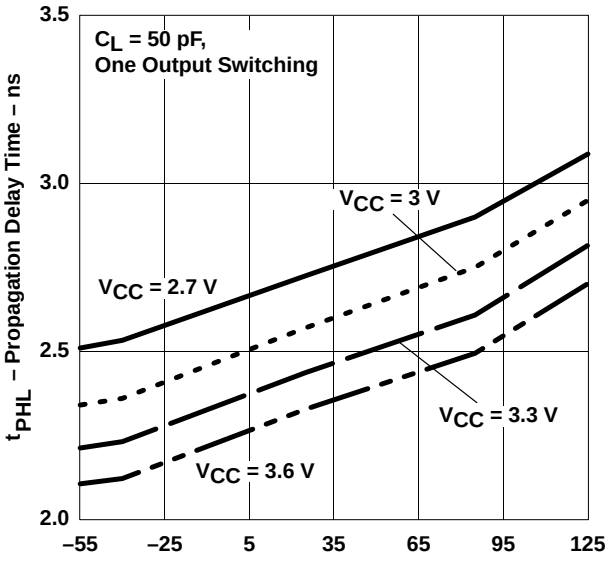
Case 3 occurs when a 5-V CMOS device drives a 3.3-V LVC device. Two different switching standards that do not match (see Figure 1) are interfacing. Upon further analysis of the 5-V CMOS V_{OH} and V_{OL} and the 3.3-V LVC V_{IH} and V_{IL} switching levels, Figure 1 shows that although a disparity exists, a 5-V tolerant 3.3-V device can function properly with 5-V CMOS input levels. With a 5-V tolerant LVC device, the configuration of a 5-V CMOS part driving a 3.3-V LVC part is possible. This configuration is not possible with an LVC device that is not 5-V tolerant.

Case 4 occurs when a 3.3-V LVC device drives a 5-V CMOS device. Two different switching standards are interfacing. As shown in Figure 1, the specified V_{OH} for a 3.3-V LVC is 2.4 V (higher output levels up to 3.3 V are possible), whereas the minimum required V_{IH} for a 5-V CMOS device is 3.5 V. As such, driving a 5-V CMOS device with a 3.3-V LVC device is impossible because, even at the maximum V_{OH} of 3.3 V, the minimum V_{IH} of 3.5 V is never attained. To accommodate this occurrence, TI is designing a series of split-rail devices; e.g., the SN74ALVCH164245 and the SN74LVC164245, which have one side of the device powered at a 3.3-V level and the other side powered at a 5-V level. By having two different power supplies on the same device, the minimum voltage levels required for switching can be met and a 3.3-V LVC can essentially drive a 5-V CMOS device.

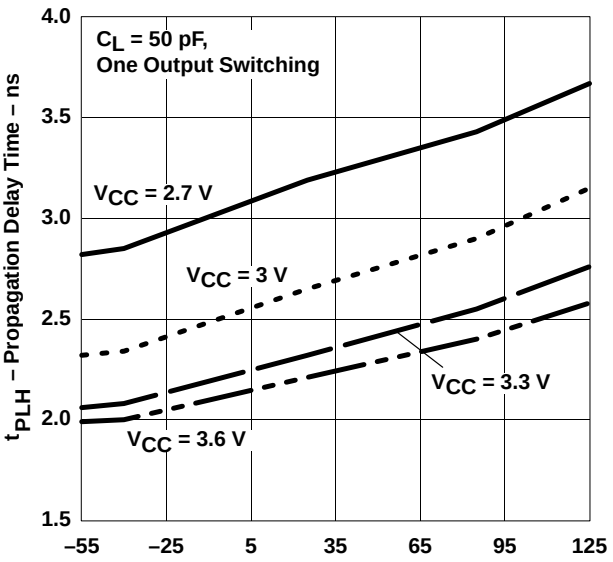
AC Performance

A desirable objective is for systems to operate at faster speeds that allow less time for performing operations. For example, consider the impact a continually increasing operating frequency has on accessing memory or on performing arithmetic computations; the faster the system runs, the less time is available for other support functions to be performed.

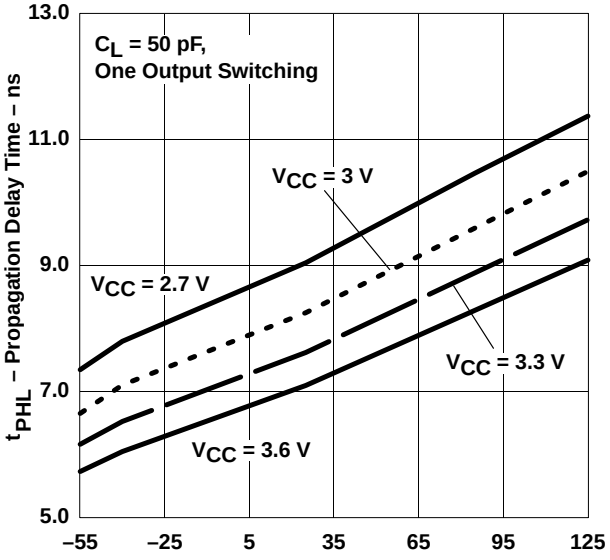
To meet this need, advances have been made in the fabrication of integrated circuits (ICs). Specifically in the low-voltage arena, the LV, LVC, ALVC, and LVT logic family fabrication geometries have undergone changes that have consistently improved their performance. This is shown in Figures 3 through 5, which compare the propagation delay times of LV, LVC, ALVC, and LVT devices for differing values of operating free-air temperature, number of outputs switching and load capacitance.



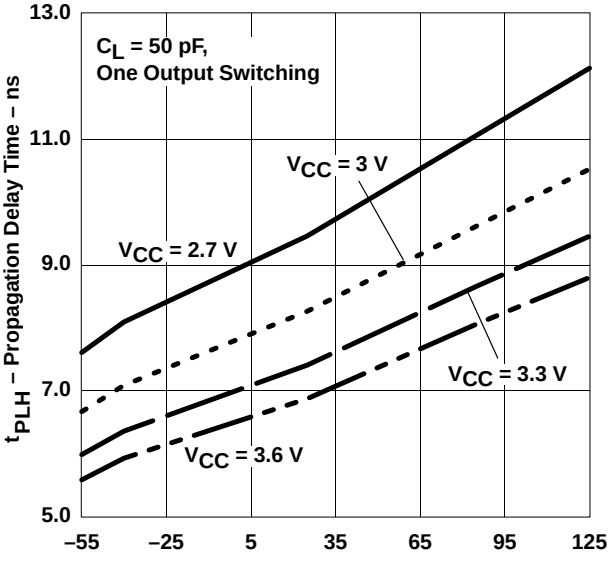
(a) SN74LVC16245A – t_{PHL}



(b) SN74LVC16245A – t_{PLH}

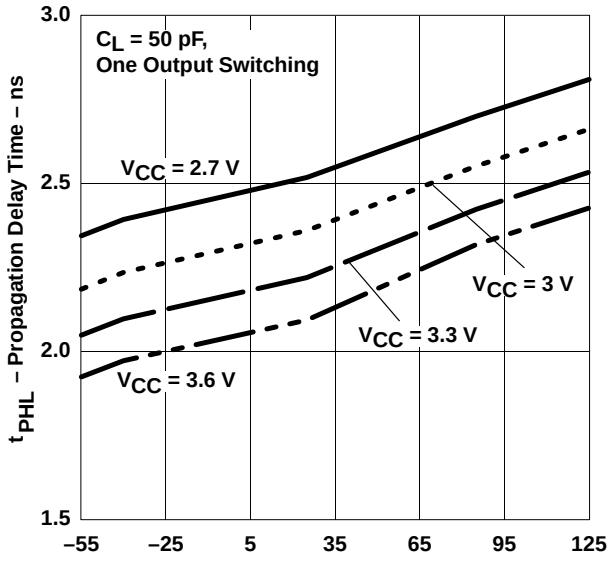


(c) SN74LV245 – t_{PHL}



(d) SN74LV245 – t_{PLH}

Figure 3. Propagation Delay Time Versus Operating Free-Air Temperature



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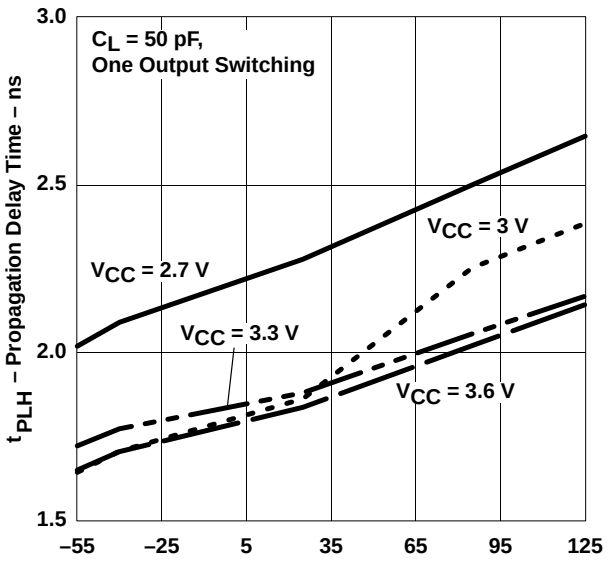
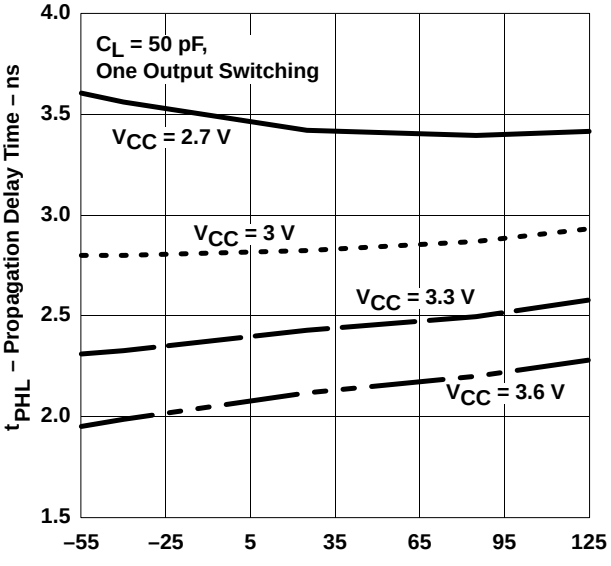
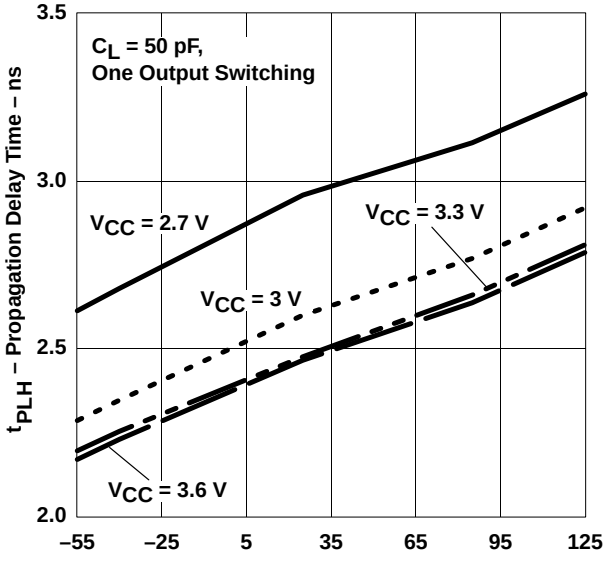


(b) SN74ALVCH16245 – t_{PLH}

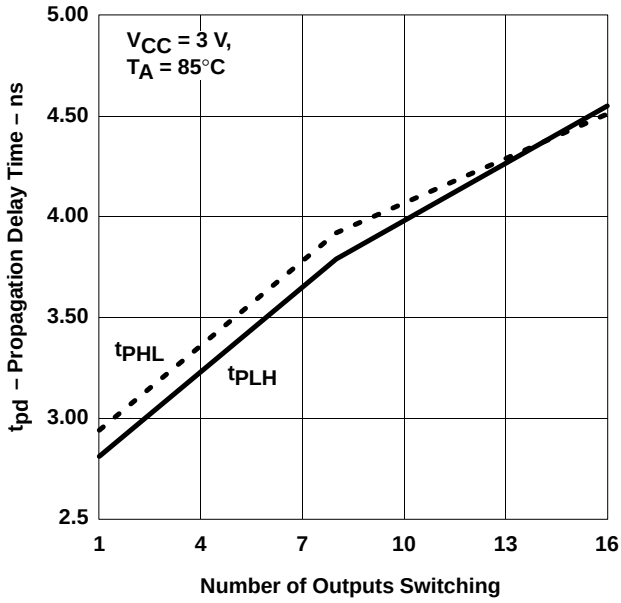


(c) SN74LVT16245 – t_{PHL}

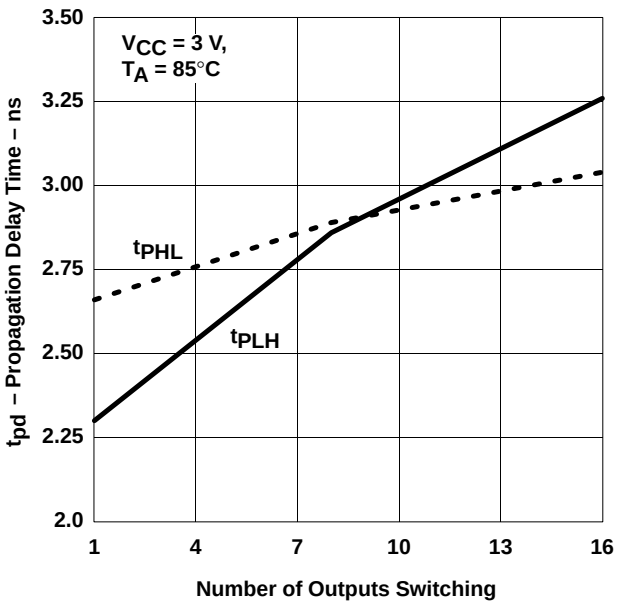


(d) SN74LVT16245 – t_{PLH}

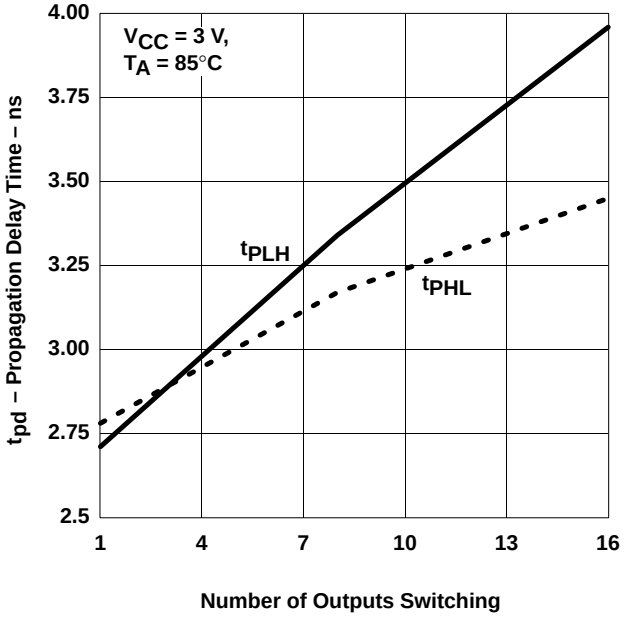
Figure 3. Propagation Delay Time Versus Operating Free-Air Temperature (Continued)



(a) SN74LVC16245A

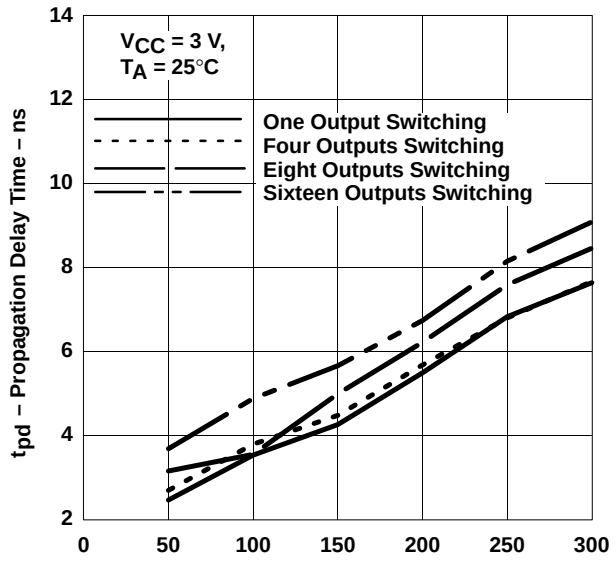


(b) SN74ALVCH16245

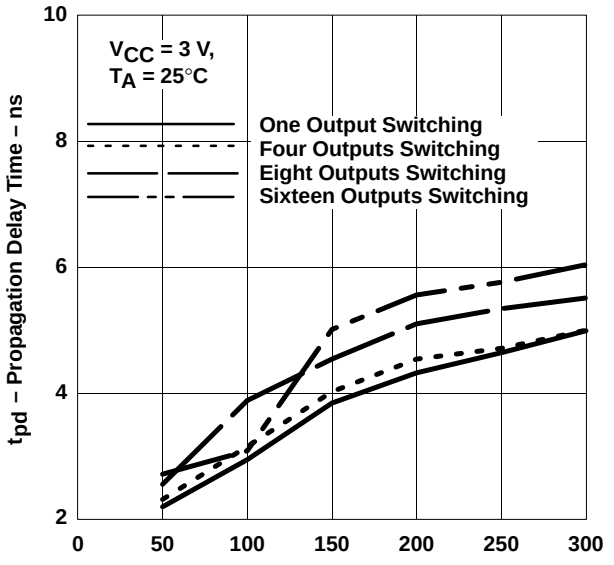


(c) SN74LVT16245

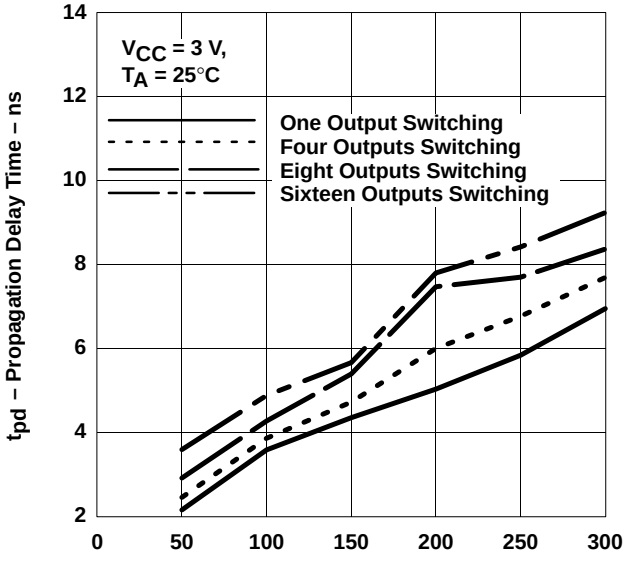
Figure 4. Propagation Delay Time Versus Number of Outputs Switching



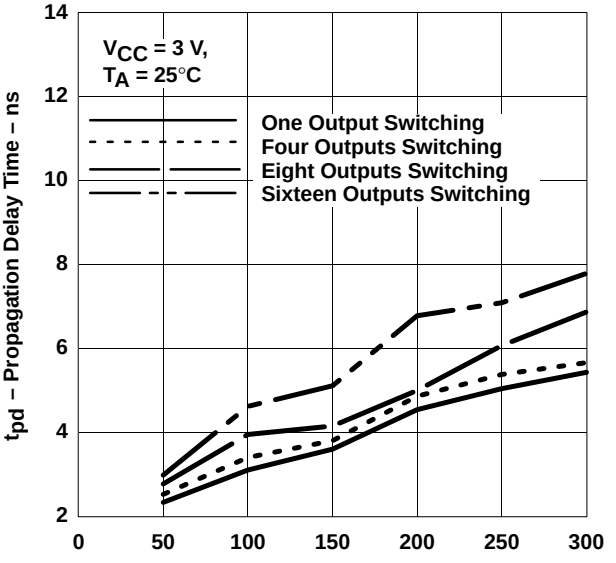
(a) SN74LVC16245A – t(PLH)



(b) SN74LVC16245A – t(PHL)



(c) SN74ALVCH16245 – t(PLH)



(d) SN74ALVCH16245 – t(PHL)

Figure 5. Propagation Delay Time Versus Load Capacitance

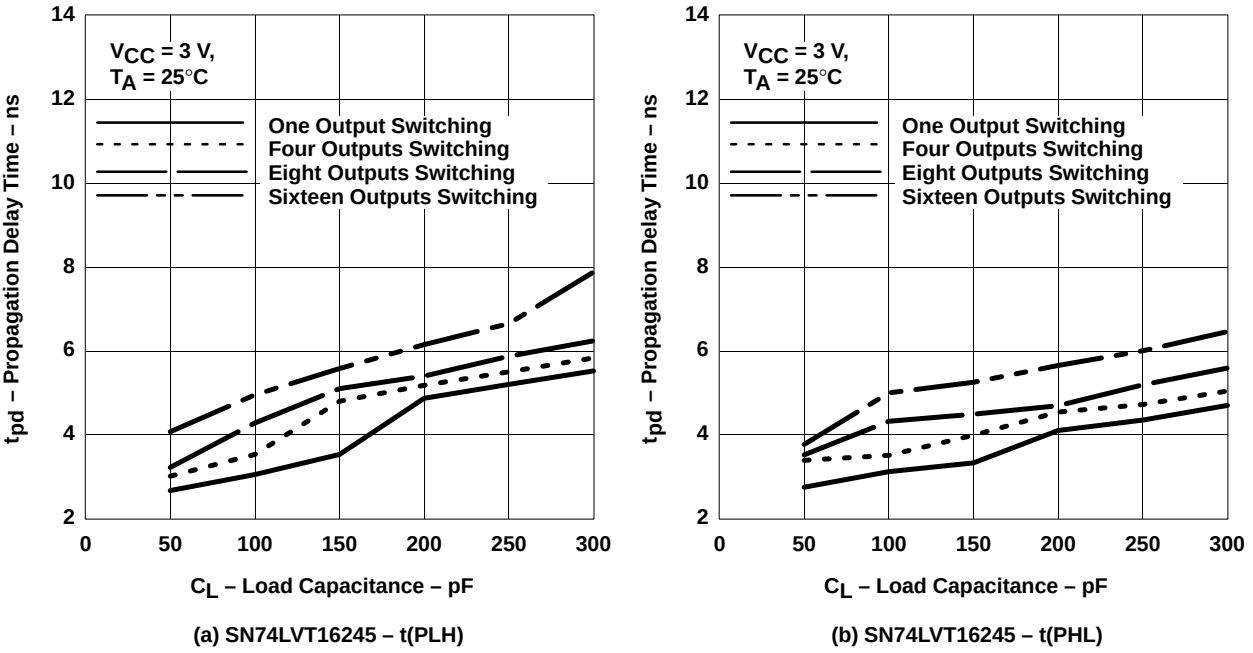


Figure 5. Propagation Delay Time Versus Load Capacitance (Continued)

Power Considerations

The general industry trend has been to make devices more robust and faster while reducing their size and power consumption. The LVC family of devices uses a CMOS output structure that has low power consumption and provides a medium drive current capability.

When calculating the amount of power consumed, both static (dc) and dynamic (ac) power must be considered. A variable when computing static power is I_{CC} and is provided in the data sheet for each specific device. The LVC family I_{CC} typically offers one-half of the LV family I_{CC}, one-fourth of the ALVC family I_{CC}, and one-nineteenth of the LVT family I_{CC}.

The majority of power consumed is dynamic due to the charging and discharging of internal capacitance and external load capacitance. The internal parasitic capacitances are known as C_{pd} and are expressed by equation 2.

$$C_{pd} = [\ (I_{CC}(\text{dynamic}) \div (V_{CC} \times f_i)\ ] - C_L \quad \textbf{(2)}$$

Where: I_{CC} = Measured value of current into the device (A)
V_{CC} = Supply voltage (V)
f_i = Input frequency (Hz)
C_L = External load capacitance (F)

When comparing the dynamic power consumed between LV, LVC, ALVC and LVT, Figure 6 shows that pure CMOS devices (the LV, LVC, and ALVC families) consume approximately the same power as BiCMOS devices (the LVT family) around the frequency of 10 MHz, but consume significantly less power as the frequency approaches 100 MHz.

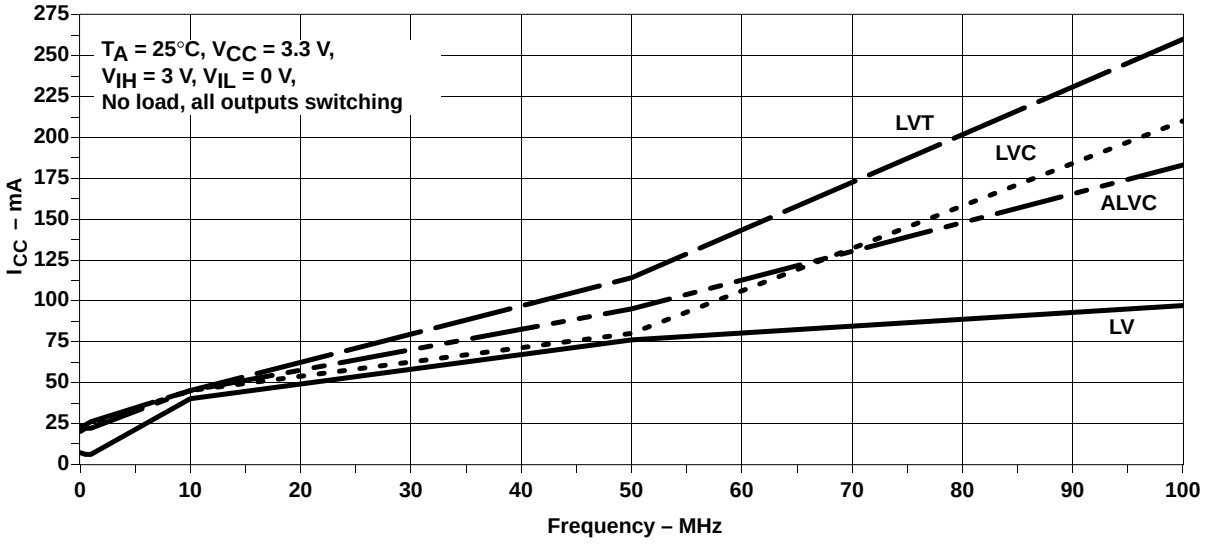


Figure 6. I_{CC} Versus Frequency

For an LVC device, the overall power consumed can be expressed by the following equation:

$$P_T = P_{(static)} + P_{(dynamic)} \quad \textbf{(3)}$$

Where: for CMOS-level inputs:

$$P_S = V_{CC} \times I_{CC}$$
$$P_D = [\ (C_{pd} + C_L) \times V_{CC}{}^2 \times f\ ]N_{SW} \quad \textbf{(4)}$$

and for TTL-level inputs:

$$P_S = V_{CC}[\ I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)\ ]$$
$$P_D = [\ (C_{pd} + C_L) \times V_{CC}{}^2 \times f\ ]N_{SW} \quad \textbf{(5)}$$

Where:
V_{CC} = Supply voltage (V)
I_{CC} = Power supply current (A)
C_{pd} = Power dissipation capacitance (F)
C_L = External load capacitance (F)
f = Operating frequency (Hz)
N_{SW} = Total number of outputs switching
N_{TTL} = Total number of outputs
ΔI_{CC} = Power supply current (A) when inputs are at a TTL level
DC_d = % duty cycle of the data (50% = 0.5)

Input Characteristics

The LVC family input structure is such that the 3.3-V CMOS dc V_{IL} and V_{IH} fixed levels of 0.8 V and 2 V are ensured, meaning that while the threshold voltage of 1.5 V is typically where the transition from a recognized low input to a recognized high input occurs (see Figure 7), it is at the levels of 0.8 V and 2 V where the corresponding output state is ensured. Additionally, a reduction in overall bus loading exists in the LVC family due to the relatively high impedance and low capacitance characteristics of CMOS input circuitry.

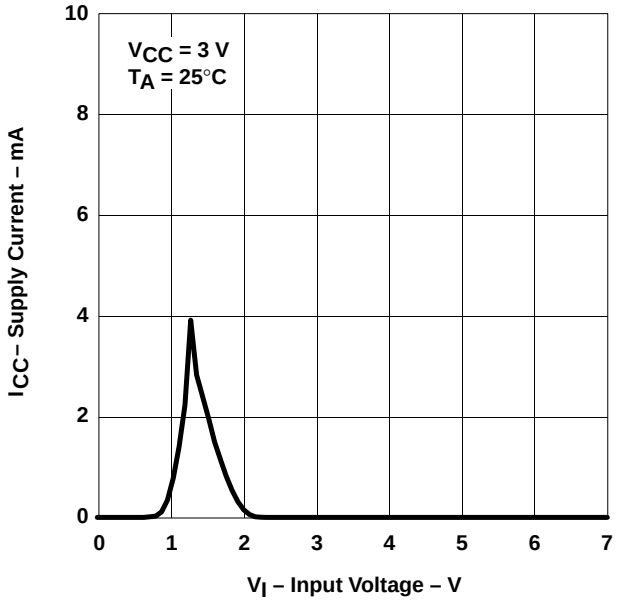


Figure 7. Supply Current Versus Input Voltage

LVC Input Circuitry

The simplified LVC input circuit shown in Figure 8 consists of two transistors, sized to achieve a threshold voltage of 1.5 V (see Figure 9). Since V_{CC} is 3.3 V and the threshold voltage is commonly set to be centered around one-half of V_{CC} in a pure CMOS input (see Figure 1), additional circuitry to reduce the voltage level is not required and the resulting simplified input structure consists of two transistors. When the input voltage V_I is low, the PMOS transistor (Q_p) turns on and the NMOS transistor (Q_n) turns off, causing current to flow through Q_p, resulting in the output voltage (of the input stage) to be pulled high. Conversely, when V_I is high, Q_n turns on and Q_p turns off, causing current to flow through Q_n, resulting in the output voltage (on the input stage) to be pulled low.

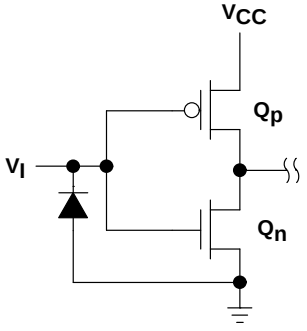


Figure 8. Simplified Input Stage of an LVC Circuit

Figure 9 is a graph of V_O versus V_I. An input hysteresis of approximately 100 mV is inherent to the LVC process geometry, which ensures the the devices are free from oscillations by increasing the noise margin around the threshold voltage.

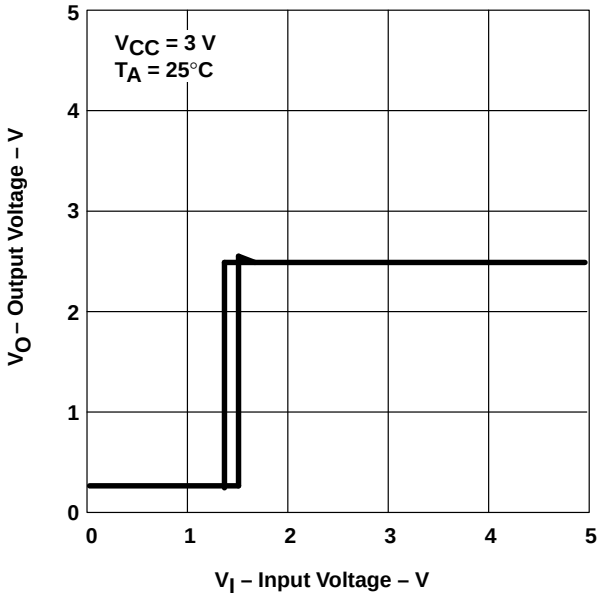


Figure 9. Output Voltage Versus Input Voltage

Figure 10 is a graph of I_I versus V_I. Additionally, the inputs of all LVC devices are 5-V tolerant and have a recommended operating condition range from 0 V to 5.5 V. If the input voltage is within this range, the functionality of the device is ensured.

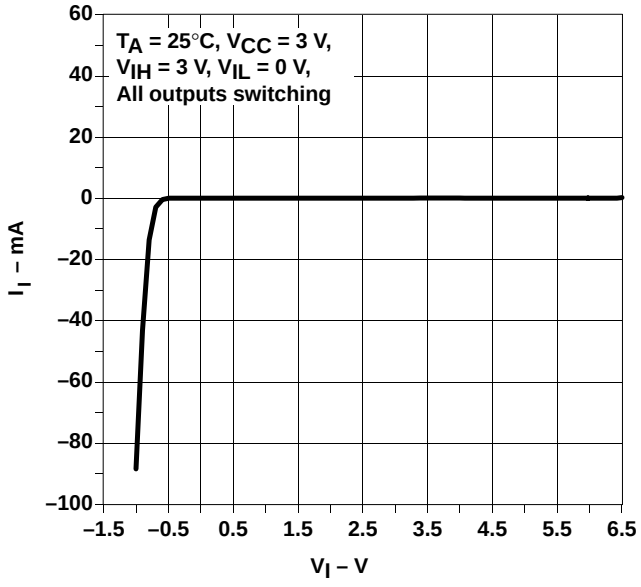


Figure 10. Input Current Versus Input Voltage

Input Current Loading

Minimal loading of the system bus occurs when using the LVC family due to the EPIC™ submicron process CMOS input structure; the only loading that occurs is caused by leakage current and capacitance. Input current is low, typically less than 100 pA, as shown in Figure 11 and Table 1. Capacitance for transceivers can be as low as 3.3 pF for C_i and 5.4 pF for C_{io}. Since both of the variables that can affect bus loading are relatively insignificant, the overall impact on bus loading on the input side using LVC devices is minimal and, depending upon the logic family being used, bus loading can decrease as a result of using LVC parts.

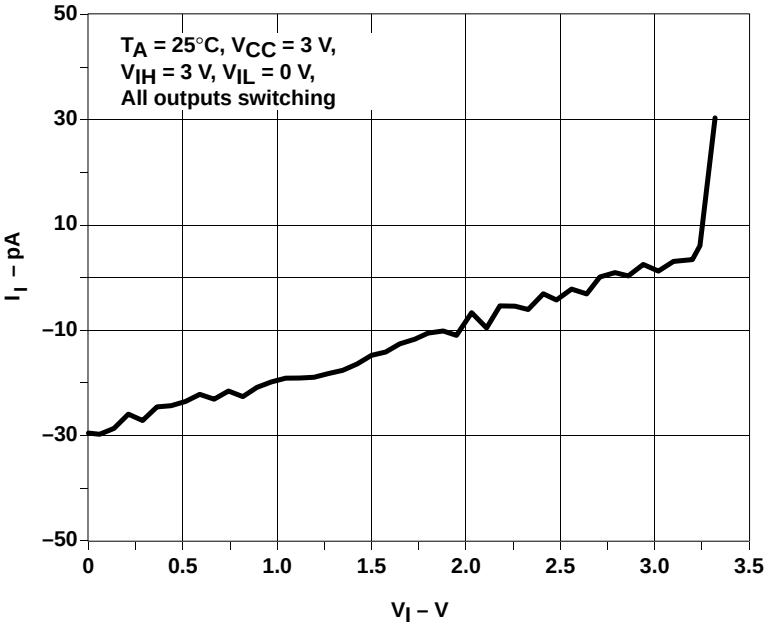


Figure 11. Input Leakage Current Versus Input Voltage

Table 1. Input-Current Specification

PARAMETER	TEST CONDITIONS		SN74LVC245A	
			MIN	MAX
I_I	V_I = 5.5 V or GND,	V_{CC} = 3.6 V		±5 µA
I_{OZ}†	V_O = V_{CC} or GND,	V_{CC} = MIN to MAX		±10 µA
I_{OZ}†	V_O = 3.6 V or 5.5 V,	V_{CC} = MIN to MAX		±50 µA

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

Supply Current Change (ΔI_{CC})

LVC devices operate using the switching standard levels shown in Figure 1. However, because the input circuitry is CMOS, an additional specification, ΔI_{CC}, is provided to indicate the amount of input current present when both p- and n-channel transistors are conducting. Although this situation exists whenever a low-to-high (or high-to-low) transition occurs, the transition occurs so quickly that the current flowing while both transistors are conducting is negligible. It is more of a concern, however, when a device with a TTL output drives the LVC part. Here, a dc current that is not at the rail, is applied to the input of the LVC device. The result is both the n-channel transistor and the p-channel transistor are conducting and a path from V_{CC} to GND is established. This current is specified as ΔI_{CC} in the data sheet for each device and is measured one input at a time with the input voltage set at V_{CC} – 0.6 V, while all other inputs are at V_{CC} or GND. Table 2 provides the ΔI_{CC} specification, which is contained in the data sheet for the SN74LVC245A.

Table 2. ΔI_{CC}-Current Specification

PARAMETER	TEST CONDITIONS	SN74LVC245A	
		MIN	MAX
ΔI_{CC}	One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND, V_{CC} = 2.7 V to 3.6 V		500 μA

Proper Termination of Unused Inputs and Bus Hold

A characteristic of all CMOS input structures is that any unused inputs should not be left floating; they should be tied high to V_{CC} or low to GND via a resistor. The value of the resistor should be approximately 1kΩ. If the inputs are not tied high or low but are left floating, excessive output glitching or oscillations can result due to induced voltage transients on the parasitic lead inductance inherent to the device input and output structure.

Implementation of the bus-hold feature on select devices is a recent enhancement to the LVC logic family. Bus hold eliminates the need for floating inputs to be tied high or low by holding the last known state of the input until the next input is present. Bus hold is a circuit composed of two back-to-back inverters with the output fed to the input via a resistor. A simplified illustration of the bus-hold circuit shown in Figure 12, and Figure 13 shows $I_{I(hold)}$ as V_I is swept from 0 to 4 V. Bus hold is beneficial because of the decreased expense of purchasing additional resistors and because it frees up limited board space.

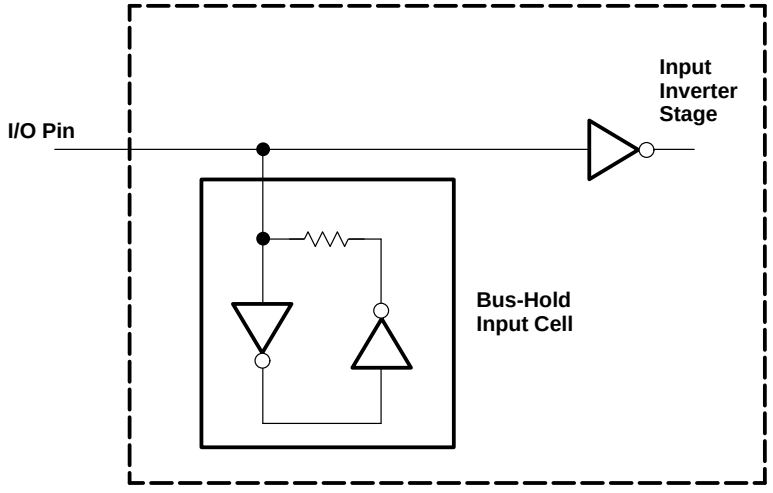


Figure 12. Bus Hold

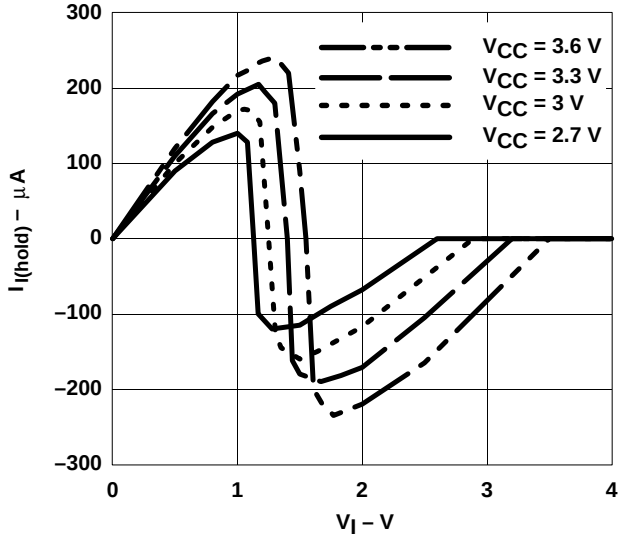


Figure 13. $I_{I(hold)}$ Versus V_I

Not all LVC devices have the bus-hold feature, but those that do are identified by the letter H added to the device name; e.g., SN74LVCH245. Additionally, any device with bus hold has an $I_{I(hold)}$ specification in the data sheet. Finally, bus hold does not contribute significantly to input current loading or output driving loading because it has a minimum hold current of 75 μA and a maximum hold current of 500 μA as shown in Table 3.

Table 3. Bus-Hold Specification [$I_{I(hold)}$]

PARAMETER	TEST CONDITIONS		SN74LVC245	
			MIN	MAX
$\Delta I_{I(hold)}$	V_I = 0.8 V,	V_{CC} = 3 V	75 μA	
	V_I = 2 V,	V_{CC} = 3 V	–75 μA	
	V_I = 0 to 3.6 V,	V_{CC} = 3.6 V		±500 μA

Output Characteristics

The LVC family uses a pure CMOS output structure. This is true of all low-voltage families except the LVT family, which uses both bipolar and CMOS circuitry. The LVC family has the dc characteristics shown in Table 4.

Table 4. LVC-Output Specification

PARAMETER	TEST CONDITIONS		SN74LVC244A		
			MIN	TYP	MAX
V_{OH}	I_{OH} = –100 μA,	V_{CC} = MIN to MAX	V_{CC} – 0.2 V		
	I_{OH} = –12 mA,	V_{CC} = 2.7 V	2.2 V		
	I_{OH} = –12 mA,	V_{CC} = 3 V	2.4 V		
	I_{OH} = –24 mA,	V_{CC} = 3 V	2.2 V		
V_{OL}	I_{OL} = 100 μA,	V_{CC} = MIN to MAX			0.2 V
	I_{OL} = 12 mA,	V_{CC} = 2.7 V			0.4 V
	I_{OL} = 24 mA,	V_{CC} = 3 V			0.55 V
I_{OZ}†	V_O = V_{CC} or GND,	V_{CC} = MIN to MAX			±10 μA
I_{OZ}†	V_O = 3.6 V to 5.5 V,	V_{CC} = MIN to MAX			±50 μA
C_o	V_O = V_{CC} or GND,	V_{CC} = 3.3 V		5 pF	

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

LVC Output Circuitry

Figure 14 shows a simplified output stage of an LVC circuit. When the NMOS transistor (Q_n) turns off and the PMOS transistor (Q_p) turns on and begins to conduct, the output voltage (V_O) is pulled high. Conversely, when Q_p turns off, Q_n begins to conduct and V_O is pulled low.

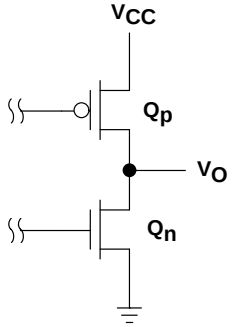


Figure 14. Simplified Output Stage of an LVC Circuit

Output Drive

Figure 15 illustrates values of I_{OL} and I_{OH} and the corresponding values of V_{OL} and V_{OH} for a typical LVC device.

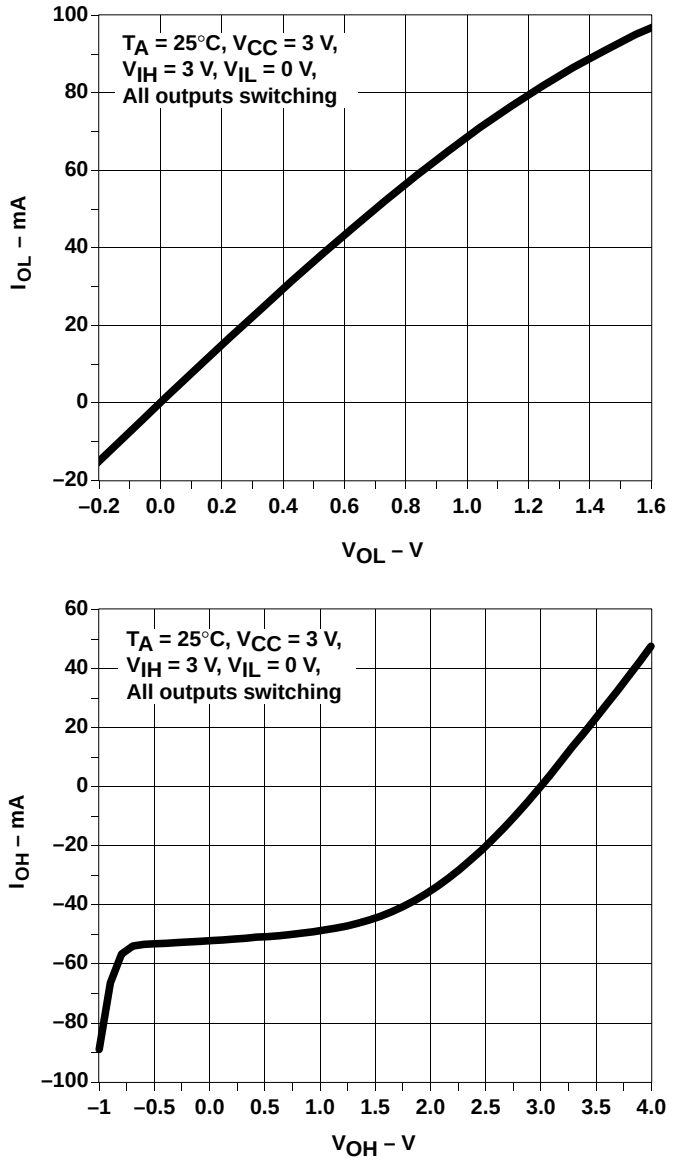


Figure 15. Typical LVC Output Characteristics

Partial Power Down

To partially power-down a device, no paths from V_I to V_{CC} or from V_O to V_{CC} can exist. With the LVC family, a path from V_I to V_{CC} has never been an issue. However, LVC devices that are not 5-V tolerant do have a path from V_O to V_{CC}. For these devices, when V_{CC} begins to diminish, a diode from V_O to V_{CC} begins to conduct and current flows, resulting in damage to the power supply and or to the device. The 5-V tolerant LVC devices are designed in such a way that this path from V_O to V_{CC} is eliminated. As such, LVC devices that are not 5-V tolerant are not capable of being partially powered down, whereas LVC devices that are 5-V tolerant are capable of being partially powered down.

Proper Termination of Outputs

Depending on the trace length, special consideration may need to be given to the termination of the outputs. As a general rule, if the trace length is less than four inches, no additional components are necessary to achieve proper termination. If the trace length is greater than four inches, reflections begin to appear on the line and the system may appear noisy and generate unreliable data. The solution to this is to terminate the outputs in an appropriate manner to minimize the reflections.

Figure 16 illustrates five different techniques for terminating the outputs. The ideal situation is to identically match the impedance (Z_O) of the trace and eliminate all reflections. In practice, however, exactly matching Z_O is not always possible and settling for a close match that adequately minimizes the reflections may be the only option.

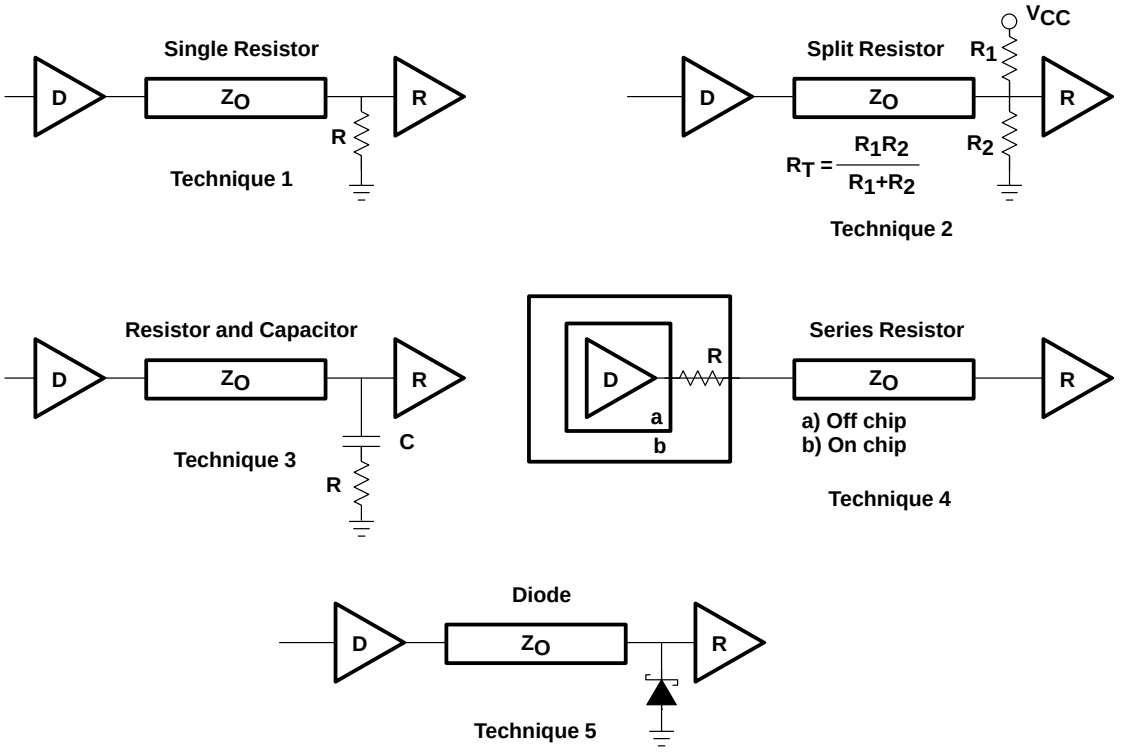


Figure 16. Termination Techniques

Technique 1 consists of a single resistor tied to GND. The ideal value of the resistor is $R = Z_O$, and the best placement for it is as close to the receiver as possible. An increase in power occurs, but no further delay is present. There is a relatively low dc noise margin in this configuration.

Technique 2 involves two split resistors; one resistor (R_1) is tied to V_{CC} and the other (R_2) is tied to GND. The ideal value of the resistors is $R_1 = R_2 = 2Z_O$; $RT = (R_1 \times R_2)/(R_1 + R_2)$, and the best placement for the resistors is as close to the receiver as possible. Technique 2 results in a heavy increase in power, with no delay being experienced, and is primarily used in backplane designs where drive current must be maintained.

Technique 3 has a capacitor in series with a resistor, both of which are running parallel to GND. The ideal value of the resistor is $R = Z_O$, and the value of the capacitor should be $60pF < C < 330$ pF. To determine the ideal value of the capacitor, it is recommended that a model simulation tool be used. The ideal placement of the resistor and capacitor is as close to the receiver as possible. Technique 3 has the highest amount of power consumed and the frequency increases, but no additional delay is experienced.

Technique 4 consists of a resistor in series with the output of the driving device and can be divided into two alternatives, depending on whether the resistor is physically located on or off the driving device. If the resistor is not located on the device, the value of the resistor should be $R = Z_O - Z_D$, where Z_D is the output impedance of the driver, and the best placement is as close to the driver as possible. Although a delay occurs, no power increase is experienced and this technique has a relatively good noise margin. If the resistor is integrated on the device and part of the chip, its value is $25 = < R = < 33\ \Omega$. This setup has a slight delay, has no increase in power, has good undershoot clamping, and is useful for point-to-point driving.

Technique 5 consists of a diode in parallel to GND that should be located as close as possible to the receiver. An increase in power is not experienced, no delay occurs, and this configuration is useful for standard backplane terminations.

Technique 5 is the most attractive of all techniques since there is no power increase and no delay occurs. However, since the delay associated with Technique 4 is so minimal and since no additional devices are required, whereas in all the other techniques at least one additional component is required, Technique 4 is usually the technique recommended by the Advanced System Logic department of Texas Instruments.

These five techniques, together with their advantages and disadvantages, are summarized in Table 5.

Table 5. Termination Techniques Summary

TECHNIQUE	ADDITIONAL DEVICES	POWER INCREASE	DELAY	IDEAL VALUE	COMMENTS
Single Resistor	1	Yes	No	$R = Z_O$	Low dc noise margin
Split Resistor	2	Significant	No	$R_1 = R_2 = 2Z_O$	Good for backplanes due to maintaining drive current
Resistor and Capacitor	2	Very significant	No	$R = Z_O$ $60 < C < 330$ pF	Increase in frequency and power
Series Resistor Off Device	1	No	Yes	$R = Z_O - Z_D$	Good noise margin
Series Resistor On Device	0	No	Small	$25 = < R = < 33\ \Omega$	Good undershoot clamping; useful for point-to-point driving
Diode	1	No	No	NA	Good undershoot clamping; useful for standard backplane terminations

Signal Integrity

System designers often are concerned with the performance of a device when the outputs are switched. The most common method of assessing this is by observing the impact on a single output when multiple outputs are switched.

Simultaneous Switching

The phenomenon of simultaneous switching can be measured with respect to GND or with respect to V_{CC}. When measuring with respect to GND, the voltage output low peak (V_{OLP}) is the impact on one quiet, logic-low output when all the other outputs are switched from high to low. The converse is true when measuring simultaneous switching with respect to V_{CC}; i.e., the voltage output high valley (V_{OHV}) is the impact on one quiet, logic-high output when all the other outputs are switched from low to high. Figure 17 shows an example of simultaneous switching with respect to V_{OLP} and V_{OHV}.

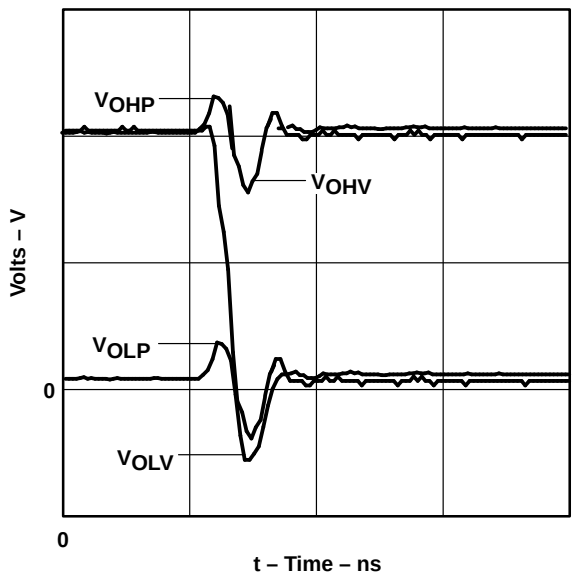


Figure 17. Simultaneous Switching Noise Waveform

One technique to reduce the impact of simultaneous switching on a device is to increase the number of power and GND pins. The strategy is to disperse them throughout the chip (see the *Advanced Packaging* section of this application report). For a complete discussion of simultaneous switching, refer to TI's *Simultaneous Switching Evaluation and Testing* application report or the *Advanced CMOS Logic Designer's Handbook*, literature number SCAA001A.

LVC Comparison to Other LVL Families

To understand where LVC is positioned relative to TI's other low-voltage families, see Figure 18, which graphs I_{OL} versus t_{pd} for LV, LVC, ALVC, and LVT. LVC is a medium-speed logic family with a medium-drive capability. Additionally, the output drive of 64 mA for the LVT family is due to the bipolar circuitry in its output stage.

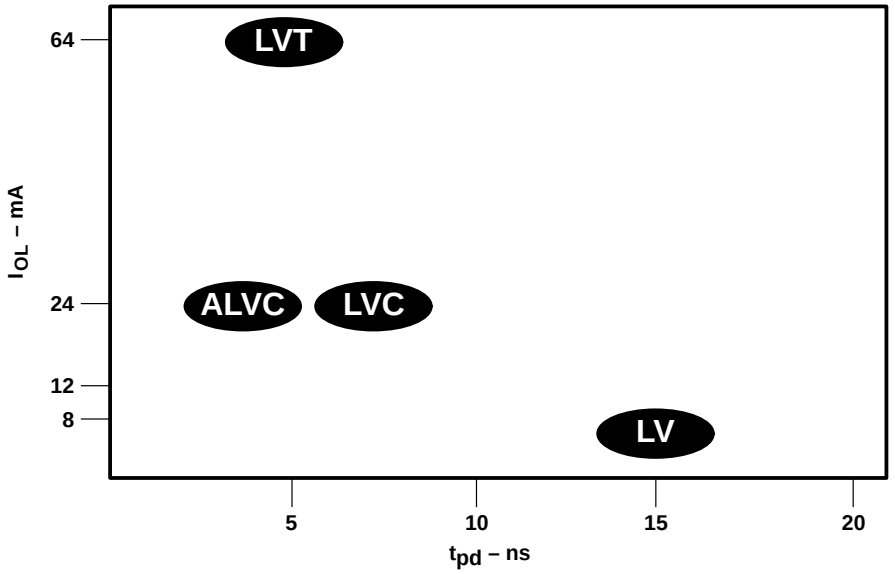


Figure 18. Low-Voltage Product Positioning

Table 6 provides a further comparison of specific family features.

Table 6. LV, LVC, ALVC, and LVT Feature Comparison

PRODUCT FAMILY		LV	LVC	ALVC	LVT
Technology		CMOS	CMOS	CMOS	BiCMOS
5-V tolerant		No	Yes	No	Yes
Octals and gates		Yes	Yes	No	No
Widebus™		No	Yes	Yes	Yes
Bus hold		No	Yes†	Yes	Yes
Damping resistors		No	Yes†	Yes†	Yes†
C_{pd}	’244	40 pF	30 pF	N/A	N/A
	’16244	N/A	20 pF	19 pF	N/A
I_{CC}	’244	20 μA	10 μA	N/A	12 mA
	’16244	N/A	20 μA	40 μA	5 mA
ΔI_{CC}	’244	500 μA	500 μA	N/A	200 μA
	’16244	N/A	500 μA	750 μA	200 μA
DC output drive		–8 mA/8 mA	–24 mA/24 mA	–24 mA/24 mA	–32 mA/64 mA
t_{pd}	’244	18 ns	6.5 ns	N/A	4.1 ns
	’16244	N/A	5.2 ns	3.6 ns	4.1 ns
C_i	’244	3 pF	3.1 pF	6 pF	4 pF
C_o	’244	8 pF	5 pF	9 pF	8 pF

† Selected functions only

SPICE Models

For information on SPICE models for the LVC family and other logic family models, consult TI's *Advanced Bus Interface SPICE I/O Models Data Book*, 1995, literature number SCBD004A.

Advanced Packaging

Figure 19 shows a comparison of the various packages in which LVC devices are available; for ease of analysis, 24-pin packages and 48-pin packages are included. (Figure 19 is not an all-inclusive list of pin counts and corresponding packages; e.g., the TSSOP package is available in both 20-pin and 24-pin format). Continued advancements in packaging are making more functionality possible with smaller space requirements.

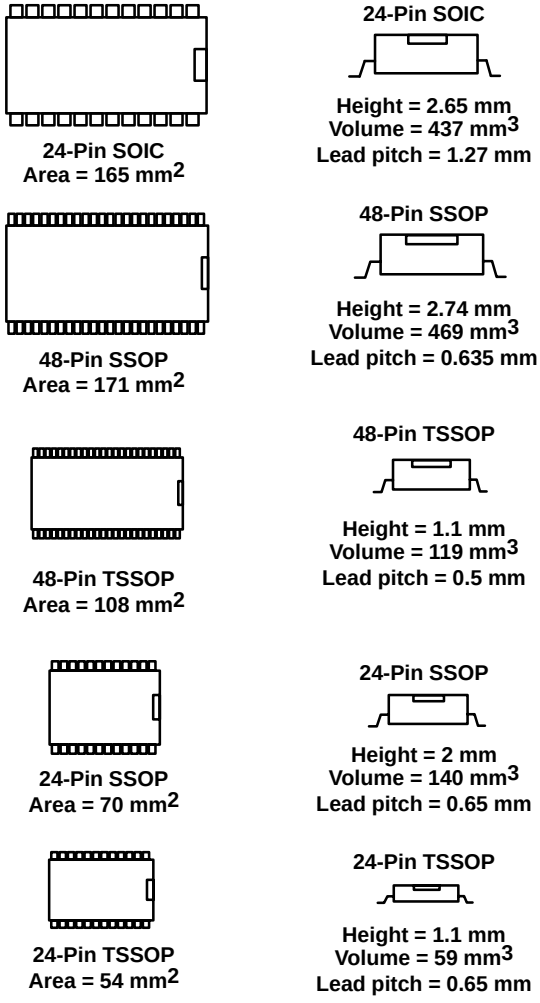


Figure 19. LVC Packages

Figure 20 shows a typical pinout structure for the 48-pin SSOP for the SN74LVC16245A. The flow-through design promotes ease of board layout and the GND and V_{CC} pins are distributed throughout the chip. This provides for simultaneous switching improvements (see the *Signal Integrity* section of this application report).

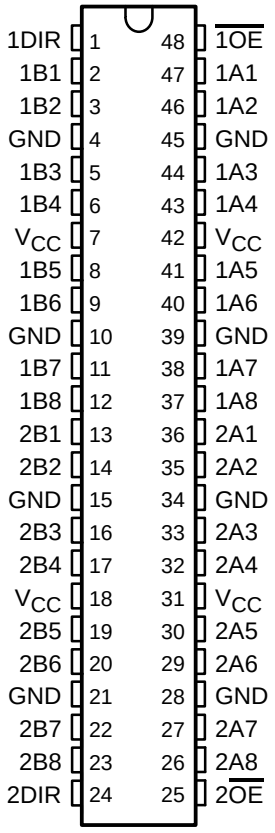


Figure 20. SN74LVC16245A Pinout

For a comprehensive listing and explanation of TI's packaging options, consult the *Semiconductor Group Package Outlines Reference Guide*, literature number SSYU001A.

Frequently Asked Questions

Question 1: *What should I do if it appears that the device is producing a noisy signal?*

Answer: The most common reason an LVC device may appear to be producing a noisy signal is if the outputs have not been terminated properly. To reduce or eliminate reflections that are inherent with long trace lengths and transmission lines, one of five techniques must be used to match the impedance of the transmission line and thereby properly terminate the output. These five techniques are: single resistor, split resistor, resistor and capacitor, series resistor, and diode. See Proper Termination of Outputs for a more detailed explanation of the techniques and the advantages and disadvantages of each method.

Question 2: *Is the LVC family 5-V tolerant?*

Answer: From an input standpoint, all of TI's LVC devices are 5-V tolerant. From an output standpoint, TI has released the most 5-V tolerant devices in the industry for the LVC (or competitor's equivalent) logic family. TI plans to release all remaining LVC 3.3-V devices in 5-V tolerant versions by the end of 1996.

Question 3: *Does the LVC family have the bus-hold feature?*

Answer: Some LVC parts have the bus-hold feature and others do not. The easiest way to determine if a particular device has bus hold is by the name of the device. If an "H" is present in the name; e.g., LVCH as opposed to LVC, then it does have bus hold. Another way to tell if bus hold has been implemented on a particular device is to examine the data sheet. If an $I_{I(hold)}$ specification is provided, then the part has bus hold.

Question 4: *Does the LVC family have built-in damping resistors on the outputs?*

Answer: Some LVC parts have built-in damping resistors and others do not. The easiest way to determine if a device has built-in damping resistors is by the name of the device. If the name has an additional 2, then the device has the built-in series damping resistors; if the name does not have an additional 2, then the device does not have them. Additionally, if the device name has an additional R as well as an additional 2, then the device in question is a bidirectional device and the series damping resistors are on both ports. (Only the series damping resistors on the output port, whether it be port A or port B, affect the operation of the device.) For example, the SN74LVC2244 is a unidirectional device that has built-in series damping resistors on the outputs, and the SN74LVCR2245 is a bidirectional device that has built-in series damping resistors on both A and B ports.

Question 5: *Can I leave unused inputs floating?*

Answer: For an LVC part that does not have the bus-hold feature, unused data inputs and outputs enable control lines must be tied high to V_{CC} or low to GND via a resistor; a resistor value of around 1 kΩ is usually recommended. If a device has the bus-hold feature, then the unused data inputs do not require being tied high or low. See question 3 to determine if a device has the bus-hold feature.

Question 6: *What is the difference between LVC and LVCH, and also ALVC and ALVCH?*

Answer: LVCH indicates that a device has the bus-hold feature, whereas a part named LVC does not. The same applies to ALVC and ALVCH. Therefore, when referring to the family as a whole, the term ALVC is used, but when referring to an individual device, the term ALVCH is used.

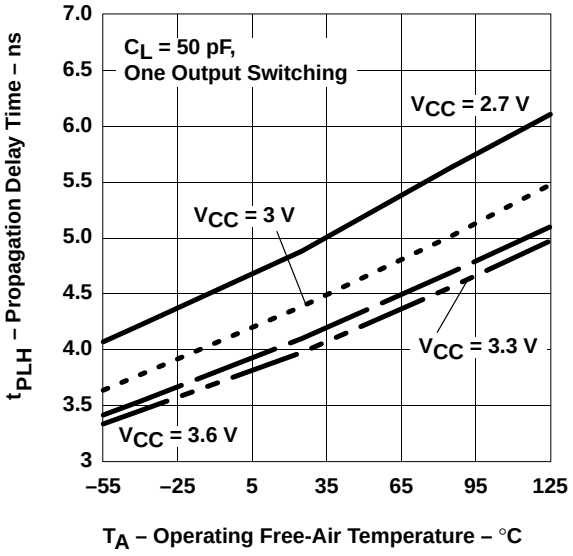
Question 7: *What is a split-rail device?*

Answer: A split-rail device has two different power supply pins on it. One side of the chip operates at V_{CCA} and the other side operates at V_{CCB}. In the LVC logic family, split-rail devices have V_{CCA} and V_{CCB} equal to 5 V and 3.3 V (this does not imply that the A port is always 5 V and the B port is always 3.3 V; they can be reversed, depending on the device).

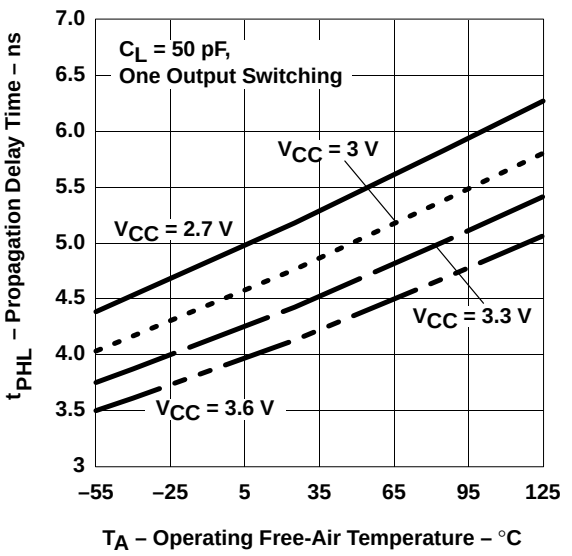
Appendix A
SN74LVCH244 Characterization Data

Propagation Delay Time Versus Temperature

Propagation Delay Time
Low-to-High-Level Output
vs
Operating Free-Air Temperature
A to Y

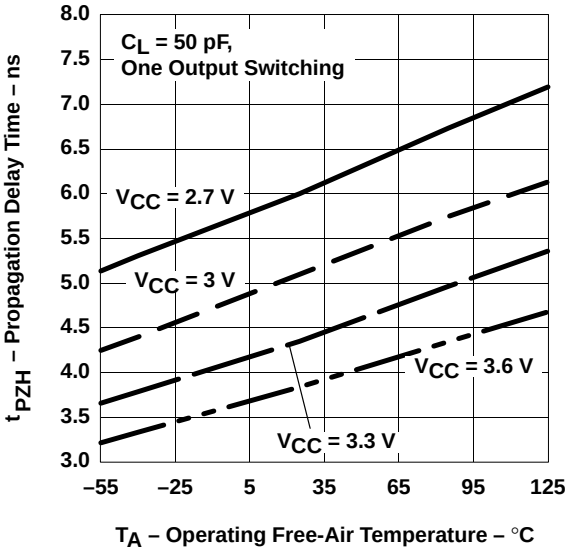


Propagation Delay Time
High-to-Low-Level Output
vs
Operating Free-Air Temperature
A to Y

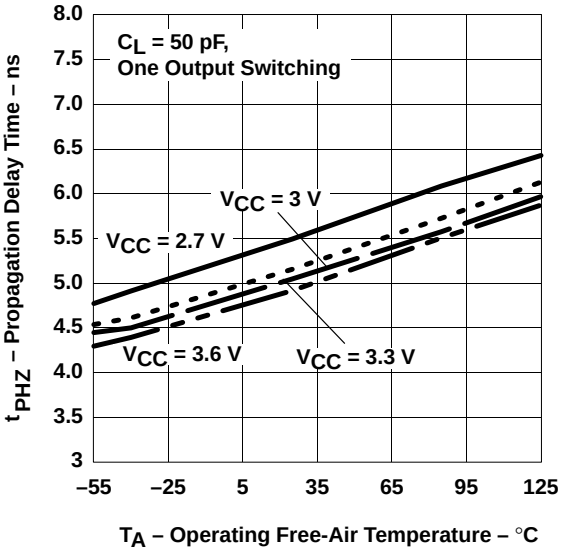


Propagation Delay Time Versus Temperature

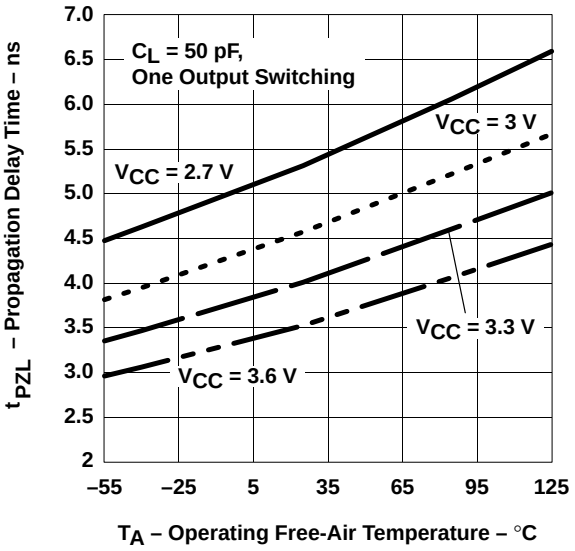
Propagation Delay Time
Enable-to-High-Level Output
vs
Operating Free-Air Temperature
$\overline{OE}$ to Y



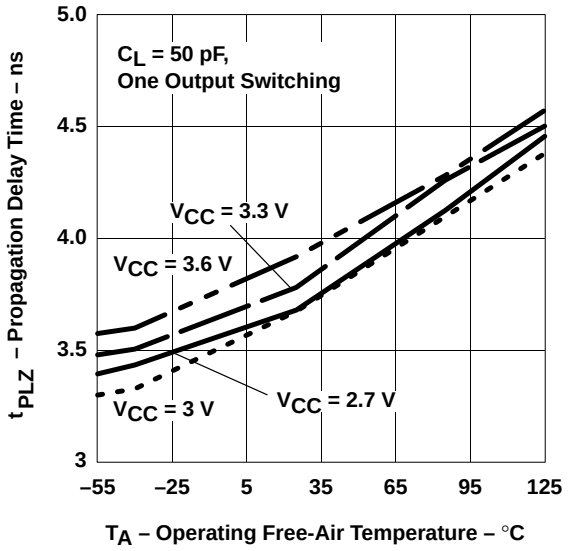
Propagation Delay Time
Disable-From-High-Level Output
vs
Operating Free-Air Temperature
$\overline{OE}$ to Y



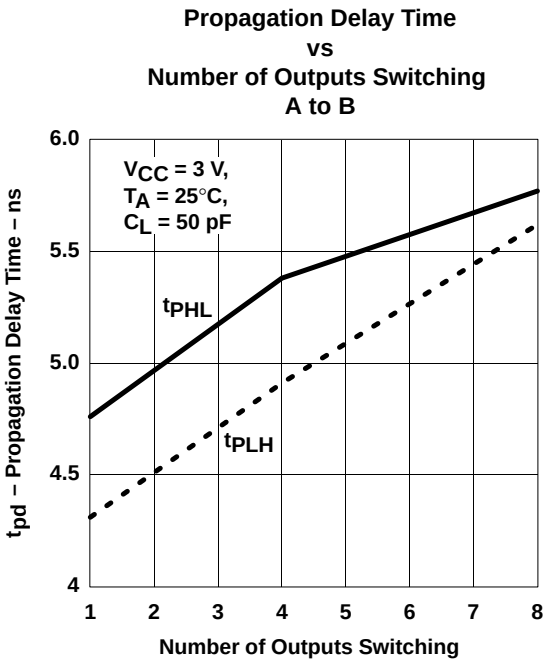
Propagation Delay Time
Enable-to-Low-Level Output
vs
Operating Free-Air Temperature
$\overline{OE}$ to Y

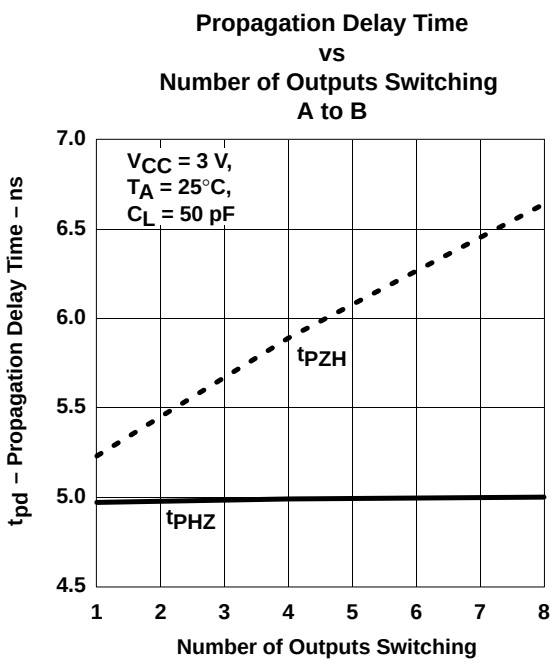


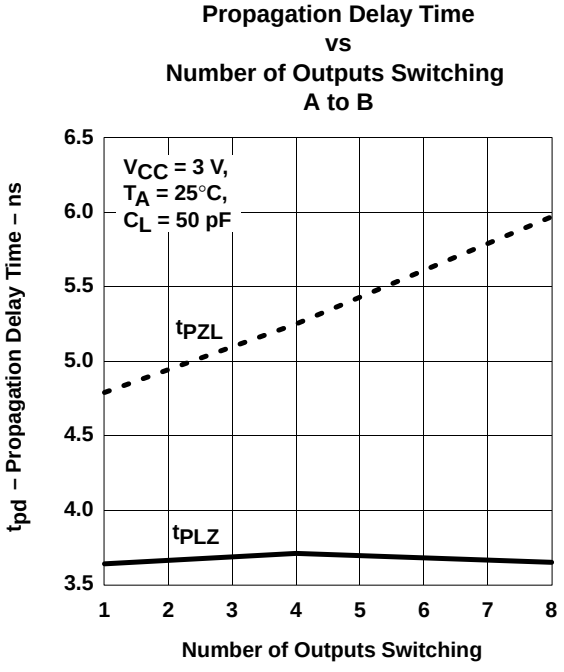
Propagation Delay Time
Disable-From-Low-Level Output
vs
Operating Free-Air Temperature
$\overline{OE}$ to Y



Propagation Delay Time Versus Number of Outputs Switching

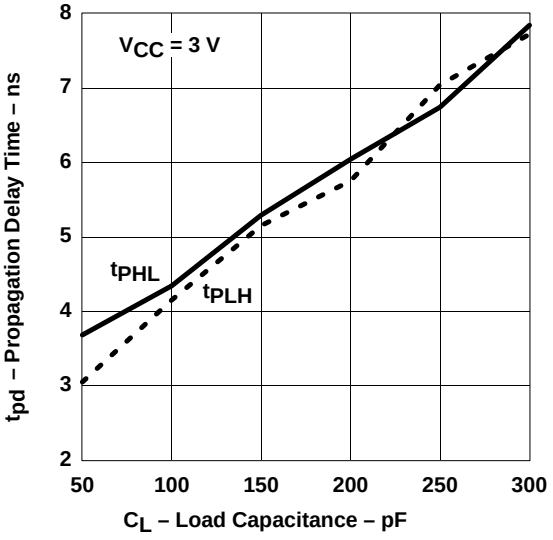




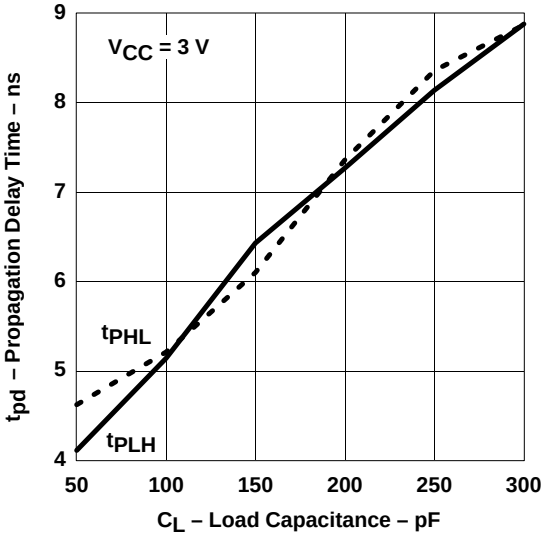


Propagation Delay Time Versus Load Capacitance

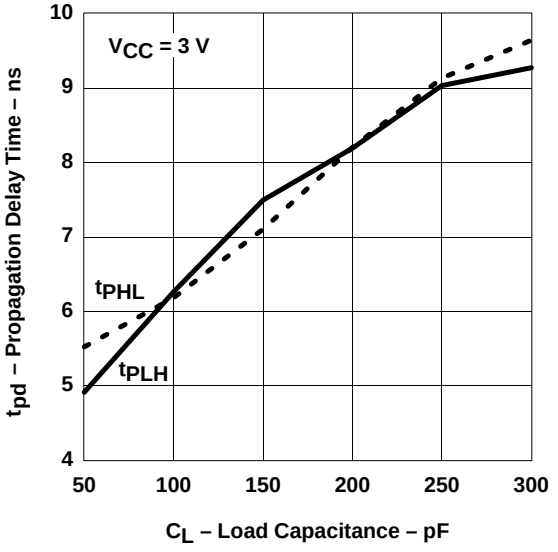
A to B
One Output Switching



A to B
Four Outputs Switching



A to B
Eight Outputs Switching



Supply Current Versus Frequency

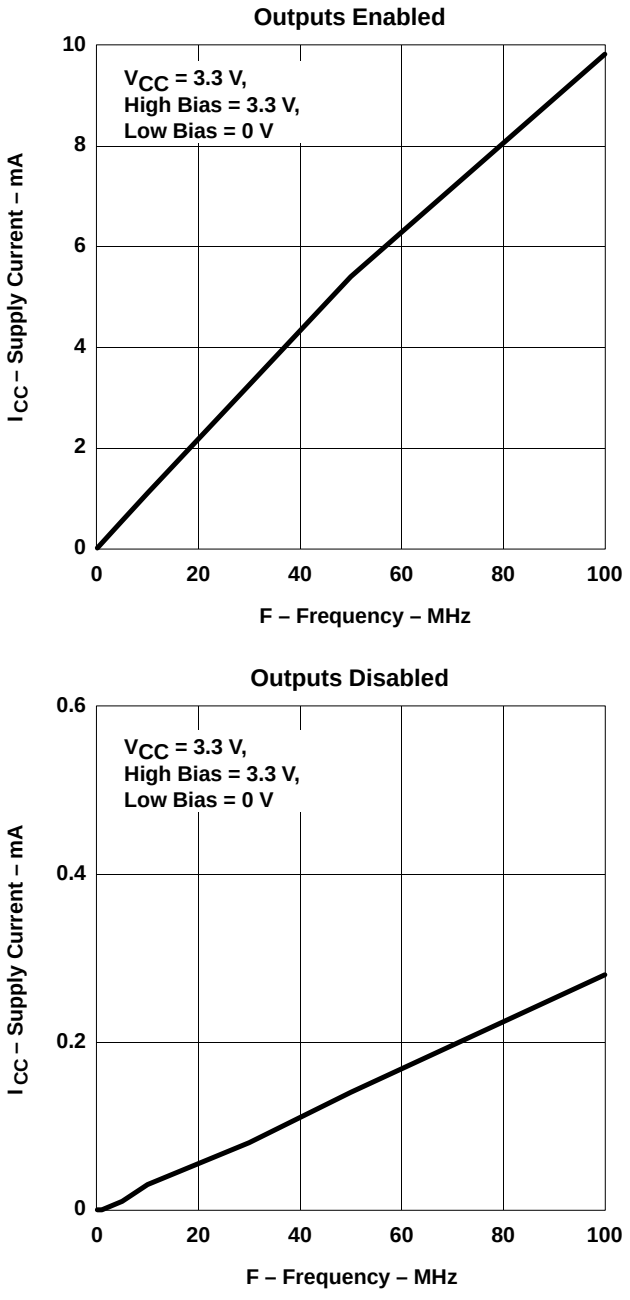


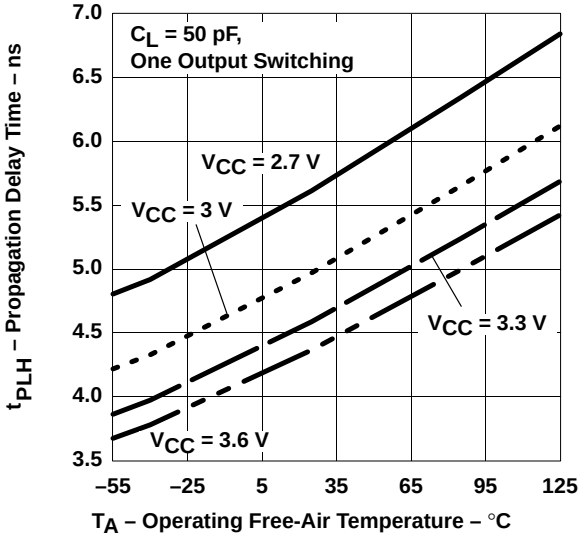
Table A–1. SN74LVCH244: Simultaneous Switching V_{OHV} and V_{OLP}

TEST	TEMPERATURE	V_{CC}	V_{OHV}	V_{OLP}
Nominal lot: one high, seven switching low to high	25°C	3.3 V	2.44 V	
Nominal lot: one low, seven switching high to low	25°C	3.3 V		0.62 V

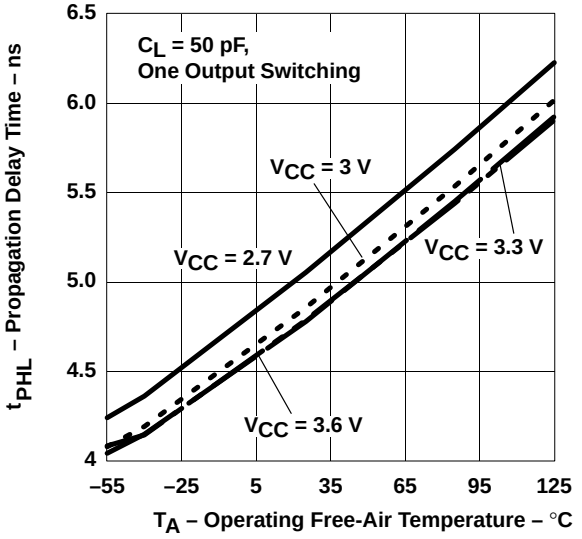
Appendix B
SN74LVC374A Characterization Data

Propagation Delay Time Versus Temperature

Propagation Delay Time
Low-to-High-Level Output
vs
Operating Free-Air Temperature
D to Q

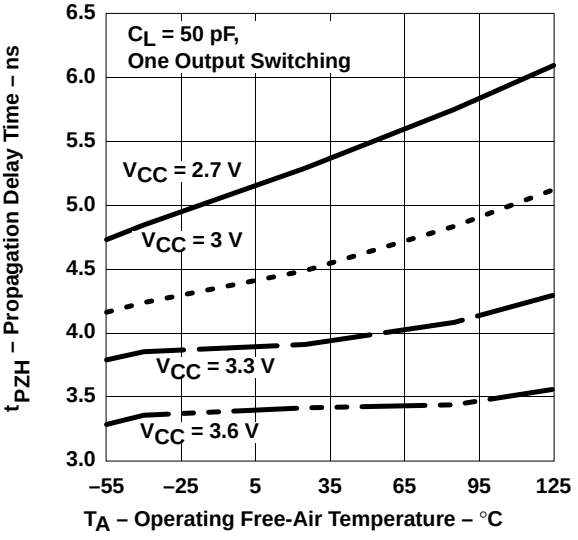


Propagation Delay Time
High-to-Low-Level Output
vs
Operating Free-Air Temperature
D to Q

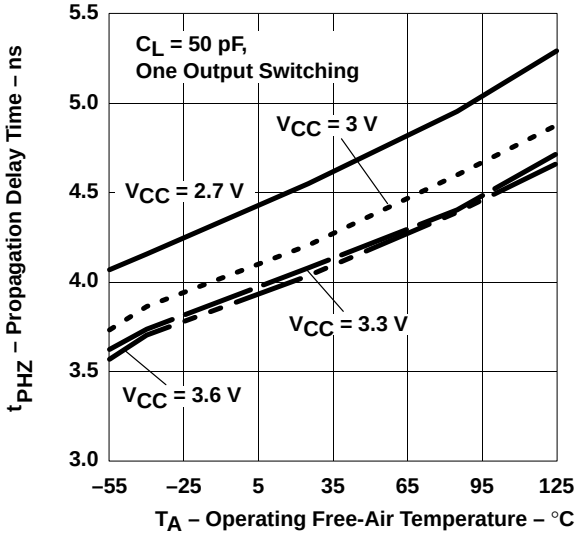


Propagation Delay Time Versus Temperature

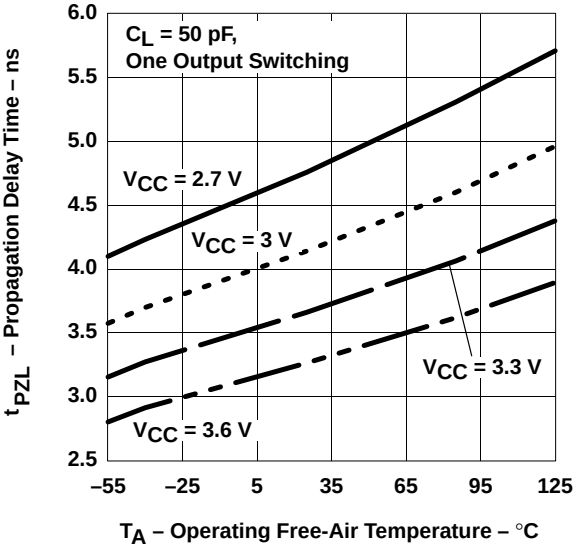
Propagation Delay Time
Enable-to-High-Level Output
vs
Operating Free-Air Temperature
OE to Q



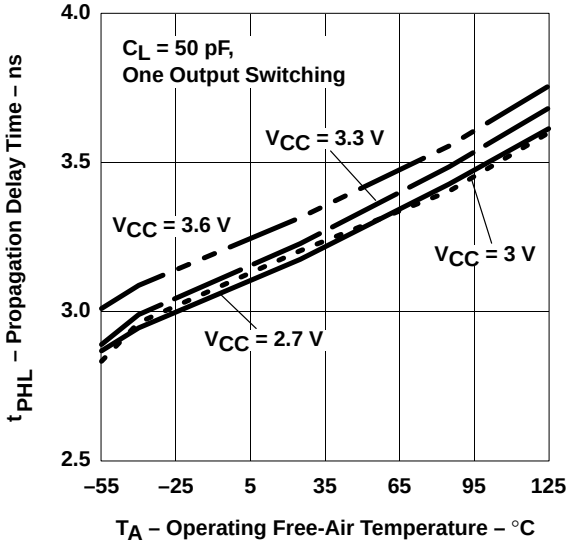
Propagation Delay Time
Disable-From-High-Level Output
vs
Operating Free-Air Temperature
OE to Q



Propagation Delay Time
Enable-to-Low-Level Output
vs
Operating Free-Air Temperature
OE to Q

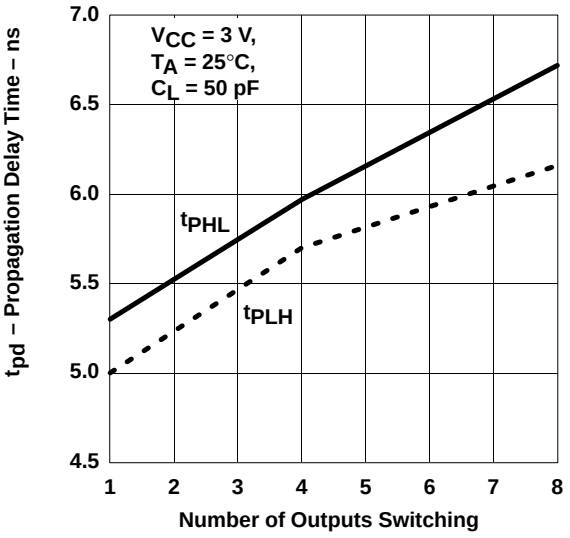


Propagation Delay Time
Disable-From-Low-Level Output
vs
Operating Free-Air Temperature
OE to Q

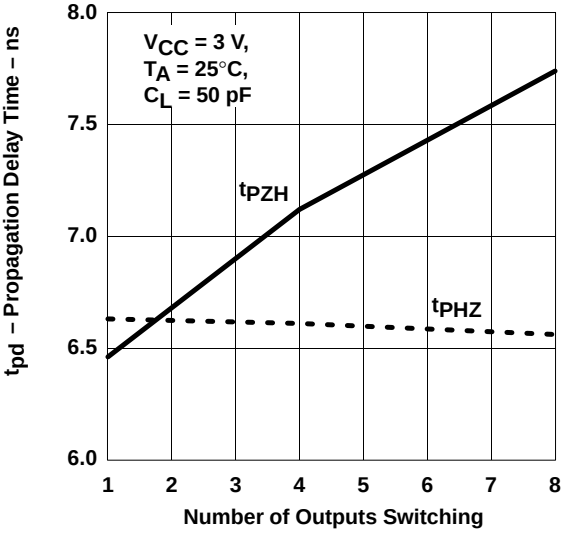


Propagation Delay Time Versus Number of Outputs Switching

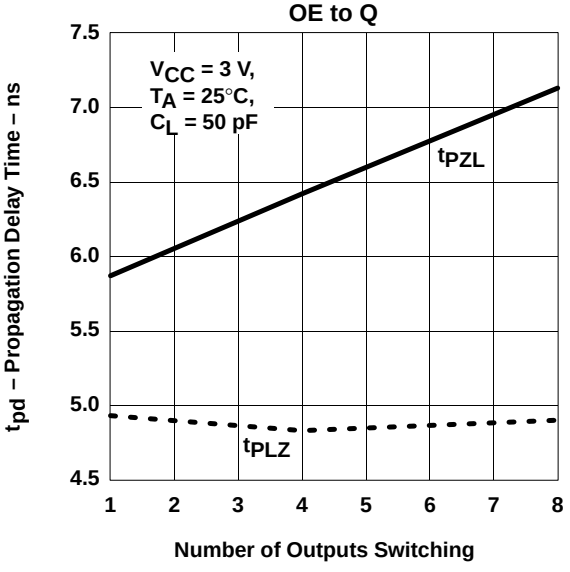
Propagation Delay Time
vs
Number of Outputs Switching
D to Q



Propagation Delay Time
vs
Number of Outputs Switching
OE to Q

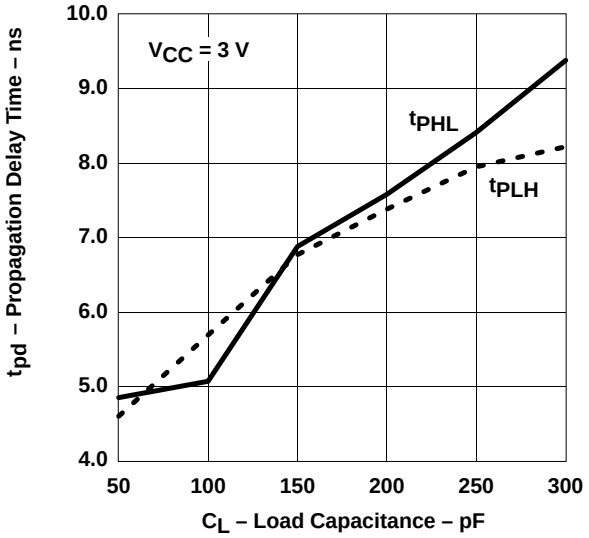


Propagation Delay Time
vs
Number of Outputs Switching
OE to Q

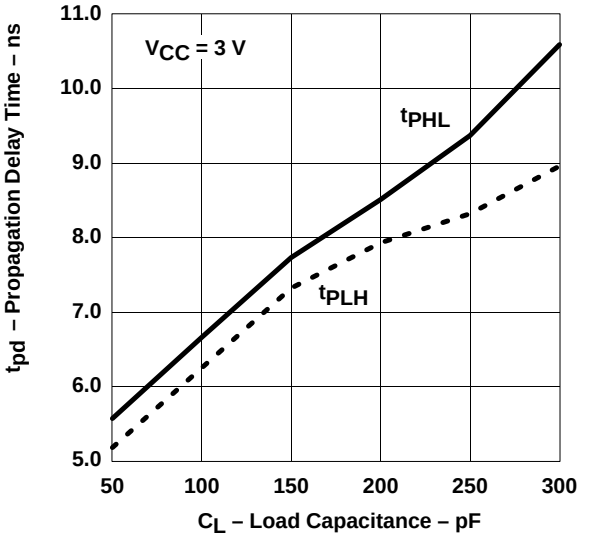


Propagation Delay Time Versus Load Capacitance

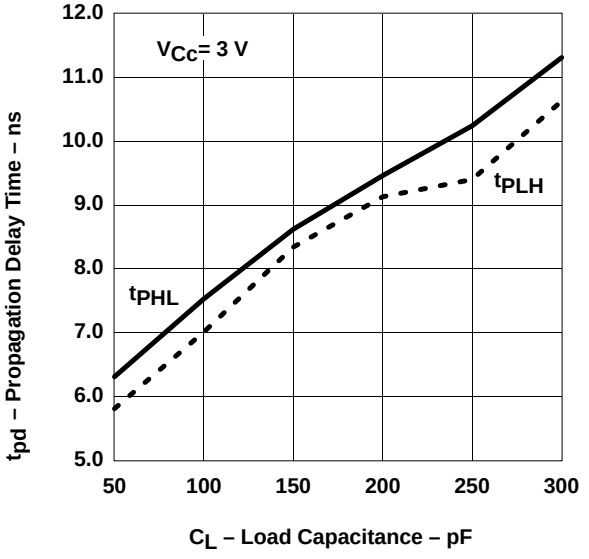
D to Q
One Output Switching



D to Q
Four Outputs Switching



D to Q
Eight Outputs Switching



Supply Current Versus Frequency

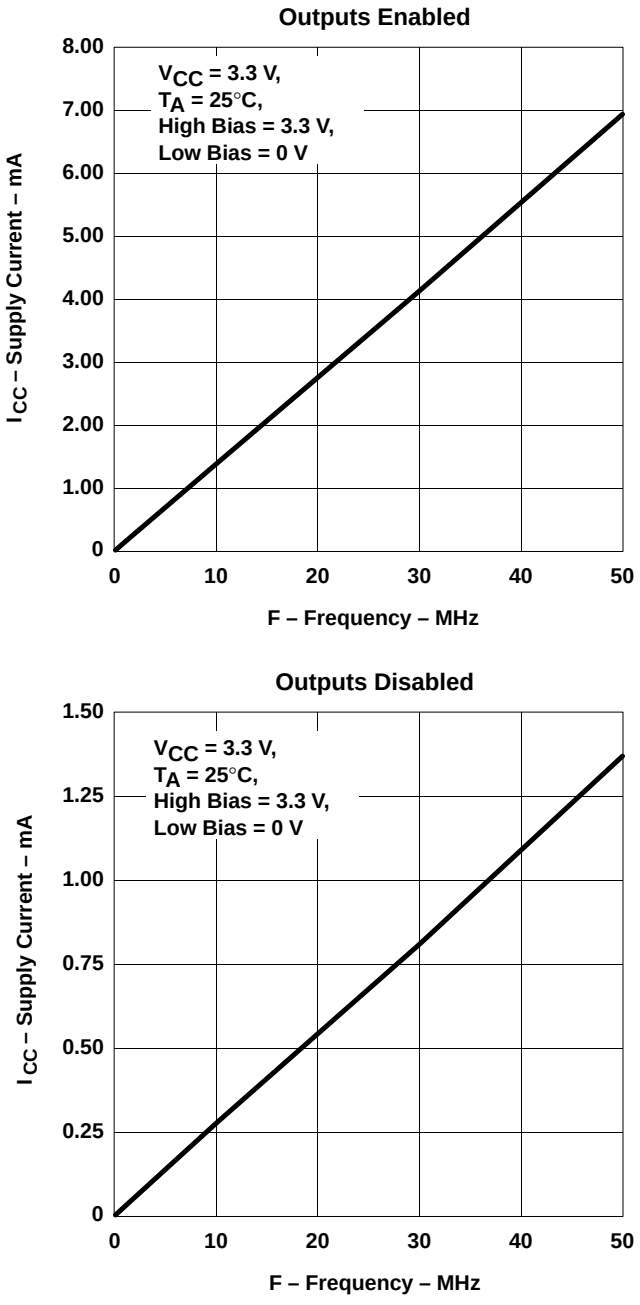


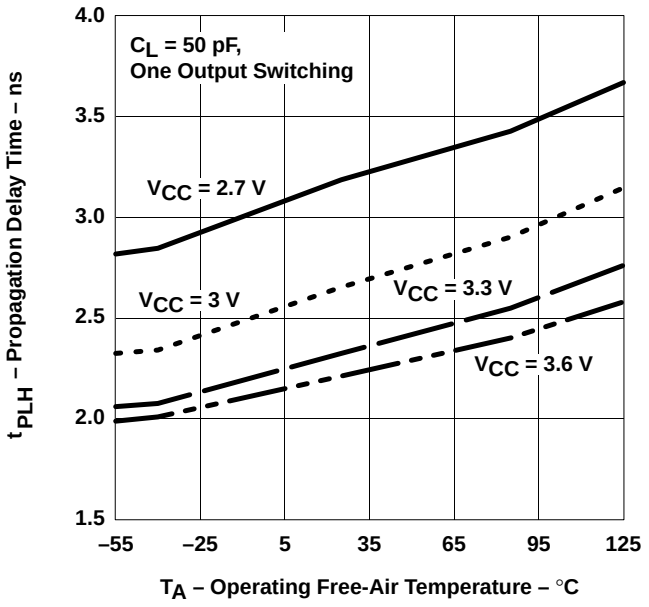
Table B–1. SN74LVC374A: Simultaneous Switching V_{OHV} and V_{OLP}

TEST	TEMPERATURE	V_{CC}	V_{OHV}	V_{OLP}
Nominal lot: one low, seven switching high to low	125°C	2.7 V		0.34 V
Nominal lot: one low, seven switching high to low	125°C	3.6 V		0.63 V
Nominal lot: one high, seven switching low to high	125°C	3.6 V	2.51 V	
Nominal lot: one low, seven switching high to low	25°C	3.3 V		0.64 V
Nominal lot: one high, seven switching low to high	25°C	3.3 V	2.46 V	

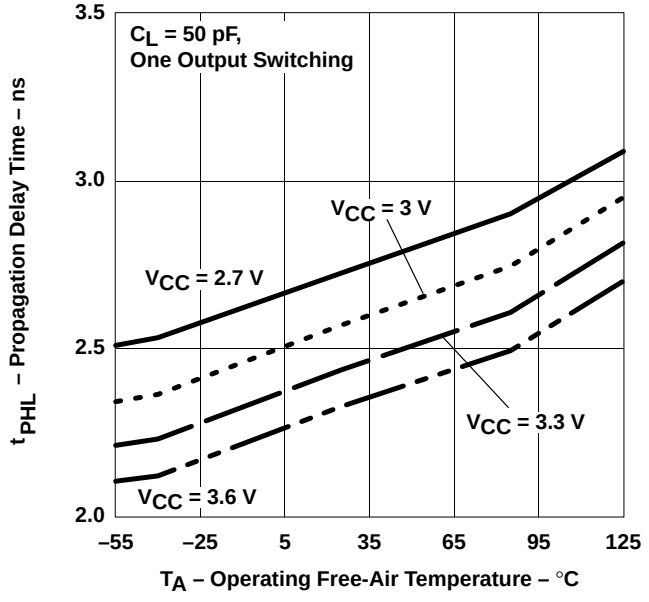
Appendix C
SN74LVC16245A Characterization Data

Propagation Delay Time Versus Temperature

Propagation Delay Time
Low-to-High-Level Output
vs
Operating Free-Air Temperature

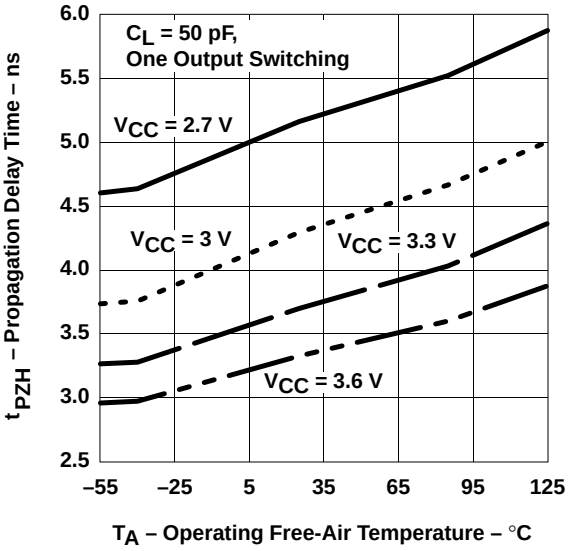


Propagation Delay Time
High-to-Low-Level Output
vs
Operating Free-Air Temperature

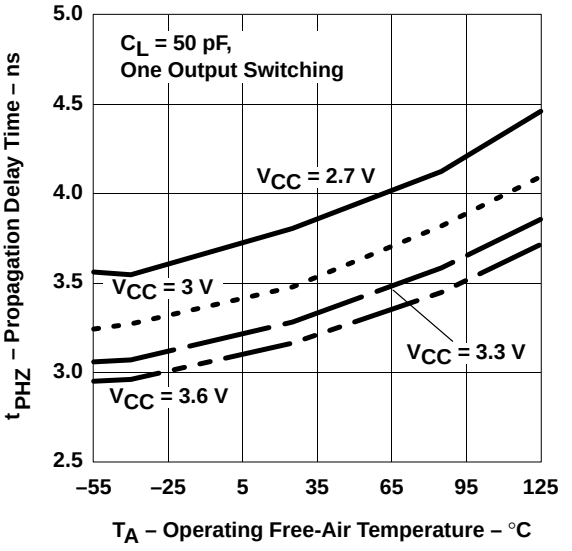


Propagation Delay Time Versus Temperature

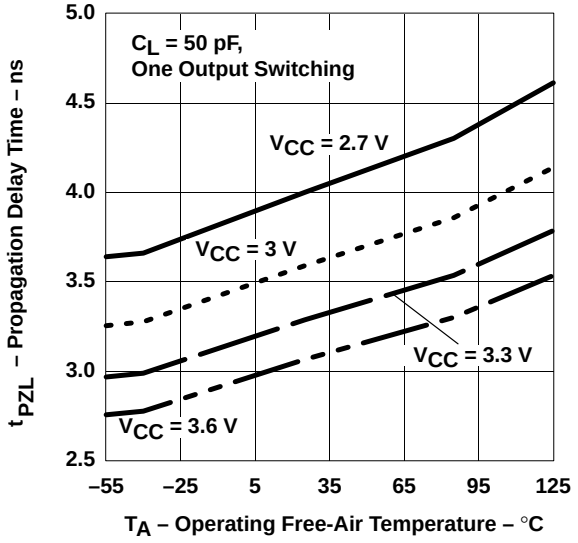
Propagation Delay Time
Enable-to-High-Level Output
vs
Operating Free-Air Temperature



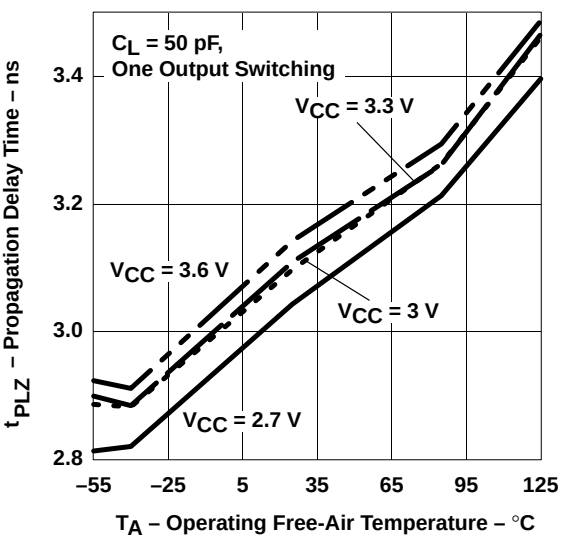
Propagation Delay Time
Disable-From-High-Level Output
vs
Operating Free-Air Temperature



Propagation Delay Time
Enable-to-Low-Level Output
vs
Operating Free-Air Temperature

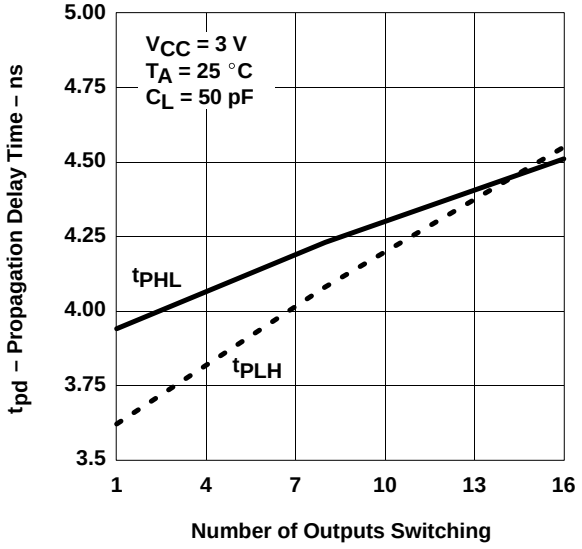


Propagation Delay Time
Disable-From-Low-Level Output
vs
Operating Free-Air Temperature

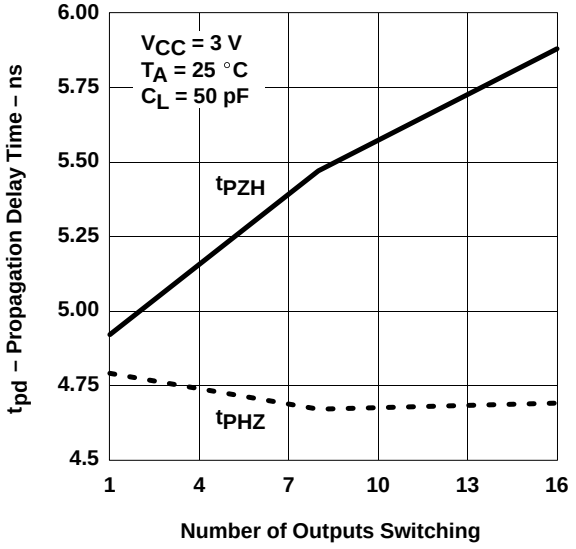


Propagation Delay Time Versus Number of Outputs Switching

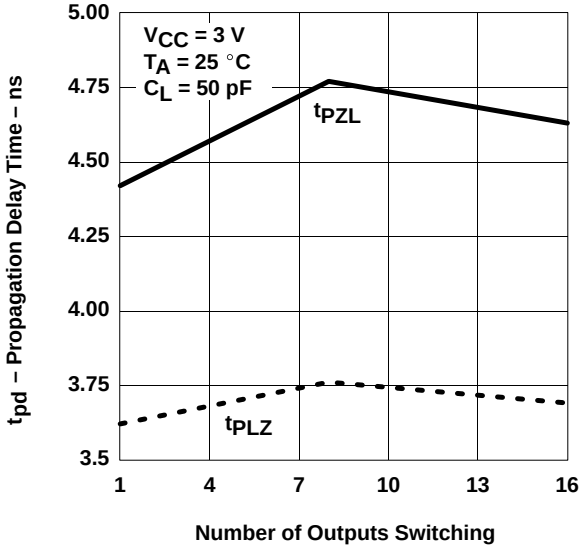
Propagation Delay Time
vs
Number of Outputs Switching
A to B



Propagation Delay Time
vs
Number of Outputs Switching
$\overline{OE}$ to B

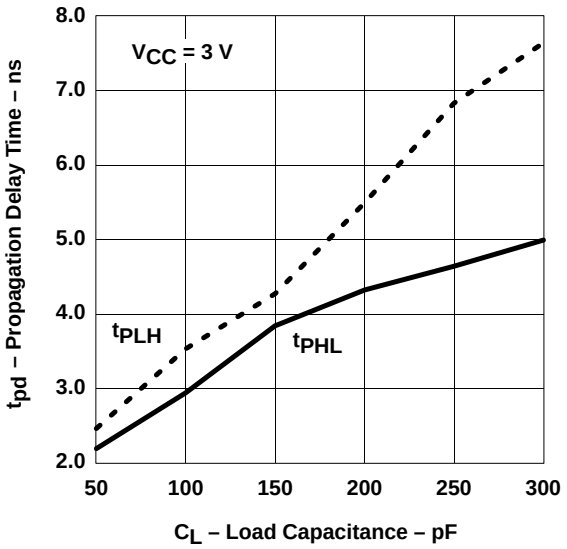


Propagation Delay Time
vs
Number of Outputs Switching
$\overline{OE}$ to B

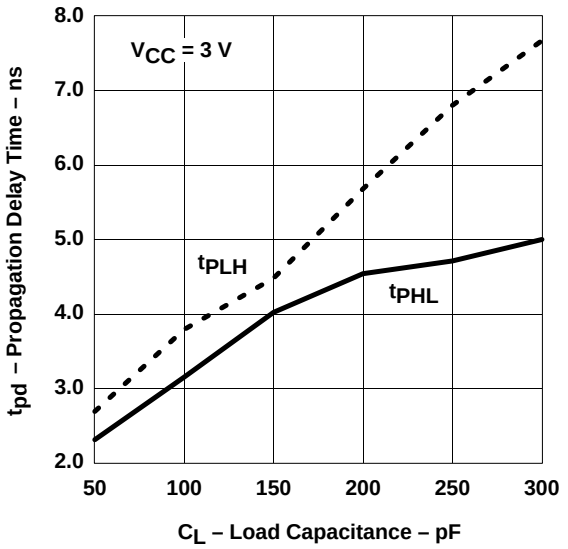


Propagation Delay Time Versus Load Capacitance

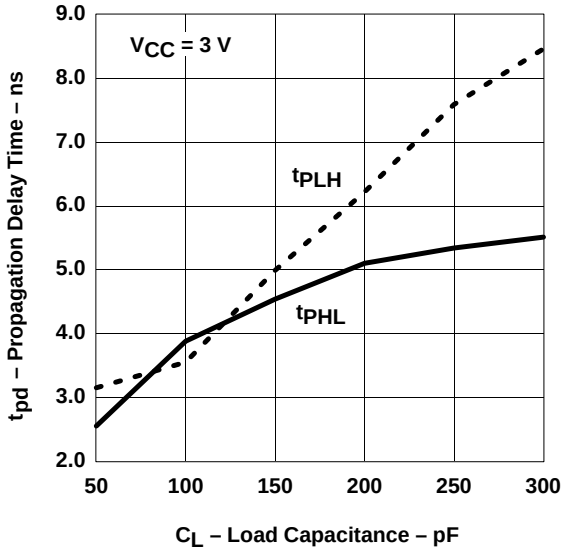
One Output Switching



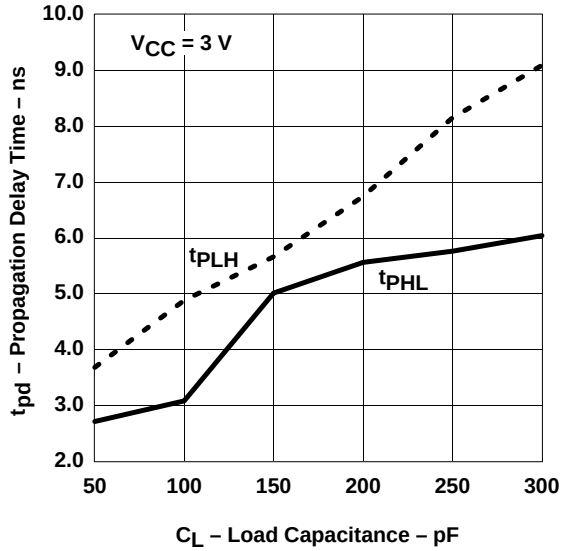
Four Outputs Switching



Eight Outputs Switching



16 Outputs Switching



Supply Current Versus Frequency

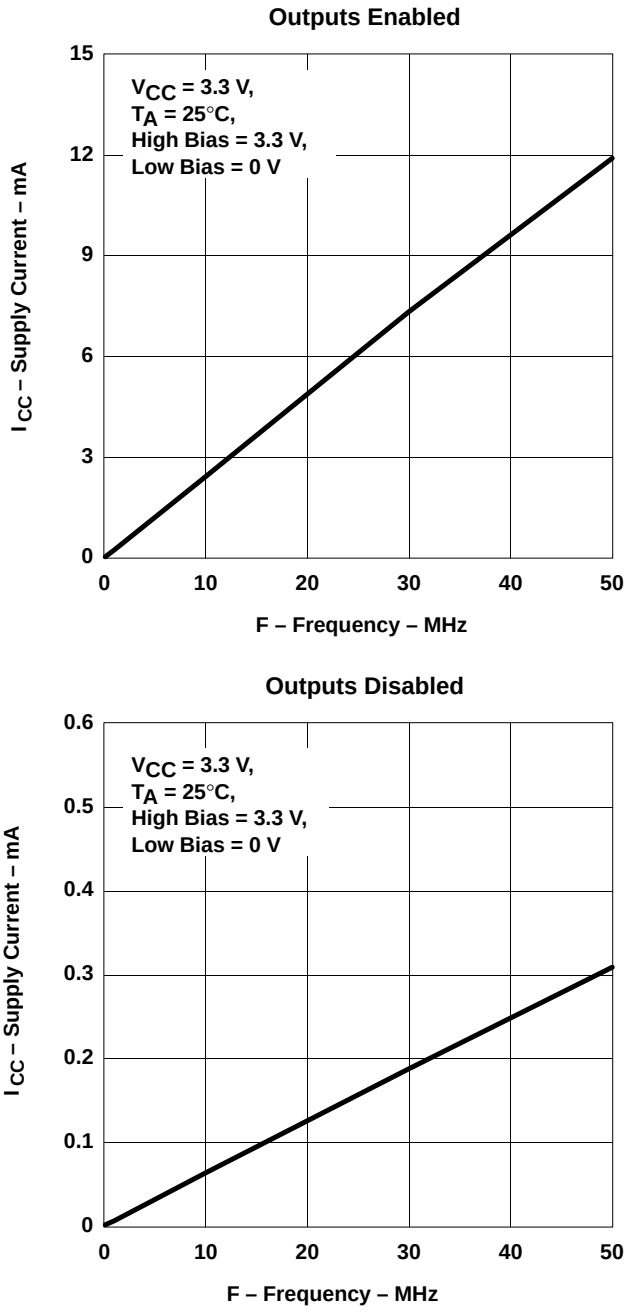


Table C–1. SN74LVC16245A: Simultaneous Switching V_{OHV} and V_{OLP}

TEST	TEMPERATURE	V_{CC}	V_{OHV}	V_{OLP}
Nominal lot: one low, seven switching high to low	125°C	3.6 V		0.56 V
Nominal lot: one high, seven switching low to high	125°C	3.6 V	2.49 V	
Nominal lot: one low, seven switching high to low	25°C	3.3 V		0.62 V
Nominal lot: one high, seven switching low to high	25°C	3.3 V	2.2 V	