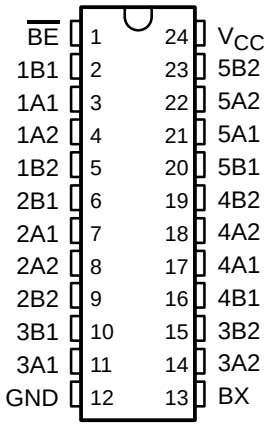
- **Functionally Equivalent to QS3388**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBTH3383 provides ten bits of high-speed TTL-compatible bus switching or exchanging with bus hold on all I/Os. The low on-state resistance of the switch allows connection to be made with minimal propagation delay. When the switch is turned off, the bus-hold circuit pulls all I/Os to V_{CC} or to GND, depending on the last-known state of the pin. The bus-hold feature holds unused buses in a known TTL state, away from threshold. The bus-hold circuit can hold the bus in the last-known state as long as its leakage does not exceed 100 μA. If the leakage on the bus exceeds this value, the bus hold switches states. The bus-hold feature is active only when the SN74CBTH3383 I/Os are in the high-impedance state.

The device operates as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when $\overline{BE}$ is low. The switches are open when $\overline{BE}$ is high. Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74CBTH3383 is available in TI's shrink small-outline (DB) and thin shrink small-outline (PW) package, which provide the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74CBTH3383 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

$\overline{BE}$	BX	1A1–5A1	1A2–5A2
L	L	1B1–5B1	1B2–5B2
L	H	1B2–5B2	1B1–5B1
H	X	Z	Z

PRODUCT PREVIEW

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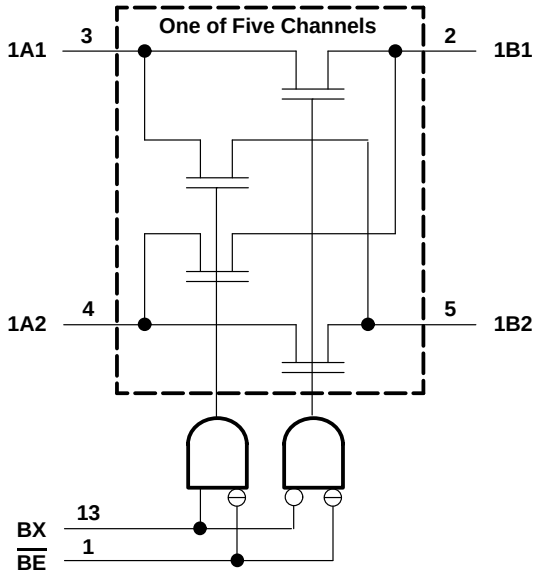
logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} to V_{DD} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package . . . . . 0.6 W
DW package . . . . . 1.6 W
PW package . . . . . 0.7 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	µA
$I_{I(hold)}$		V_{CC} = 4.5 V,	V_I = 2 V or 0.8 V		100		500	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{BE}$ = V_{CC}			6		pF
r_{on}§		V_{CC} = 4 V,	V_I = 2.4,	I_I = 15 mA		16	22	Ω
		V_{CC} = 4.5 V,	V_I = 0,	I_I = 64 mA		5	7	Ω
			V_I = 0,	I_I = 30 mA		5	7	Ω
			V_I = 2.4 V,	I_I = 15 mA		10	15	Ω

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the input terminal and the output terminal at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two terminals.

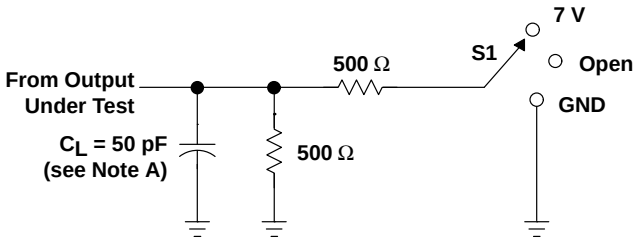
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ±0.5 V		V_{CC} = 4 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.25		0.25	ns
t_{en}	BX	A or B					ns
t_{en}	$\overline{BE}$	A or B					ns
t_{dis}	$\overline{BE}$	A or B					ns

¶ This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

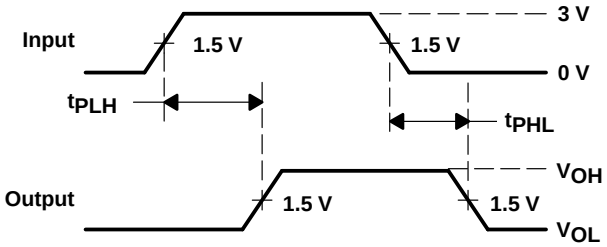
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

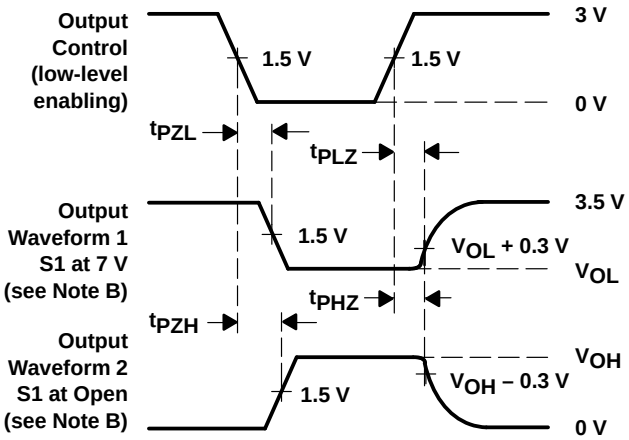


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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