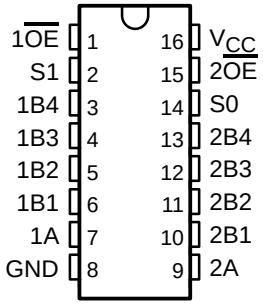
- **Functionally Equivalent to QS3253**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Quarter-Size Small-Outline (DBQ), and Thin Shrink Small-Outline (PW) Packages**

D, DB, DBQ, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3253 is a dual 4-bit to 1-bit high-speed TTL-compatible FET multiplexer/ demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

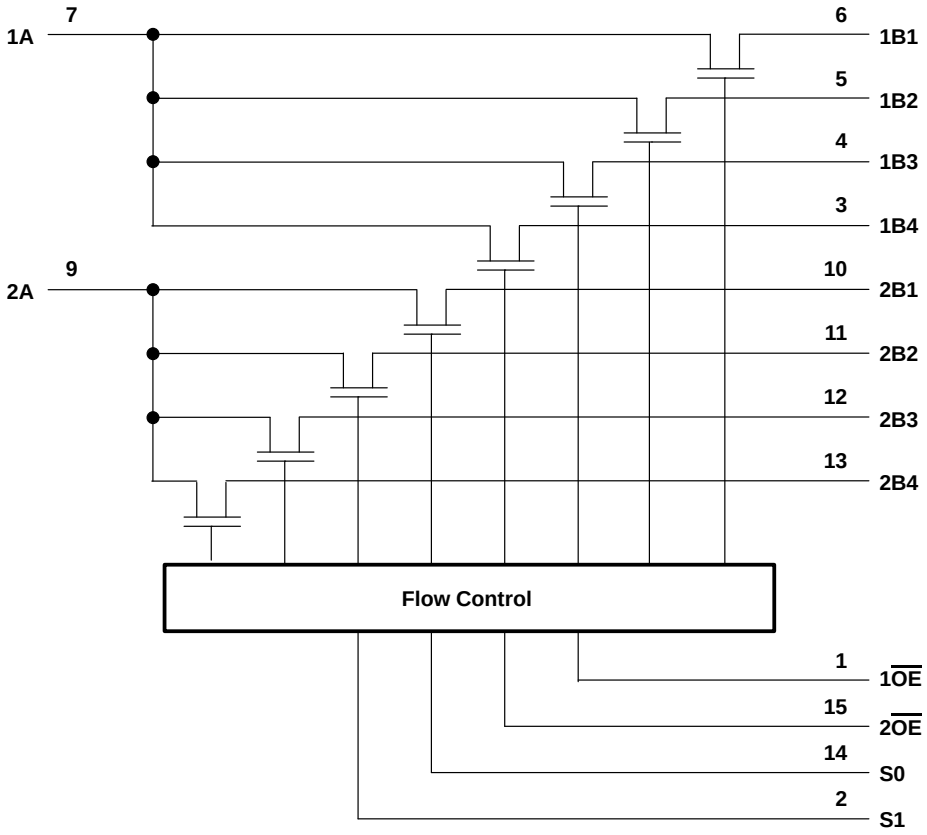
$1\overline{OE}$, $2\overline{OE}$, S0, and S1 select the appropriate B output for the A-input data.

The SN74CBT3253 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

S1	S0	$1\overline{OE}$	$2\overline{OE}$	FUNCTION
X	X	X	H	Disconnect 1A
X	X	H	X	Disconnect 2A
L	L	L	L	A = B1
L	H	L	L	A = B2
H	L	L	L	A = B3
H	H	L	L	A = B4

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_K ($V_{I/O} < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
DBQ package . . . . . 139°C/W
PW package . . . . . 149°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			10		pF
	B port					4		
r_{on}§		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA				Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

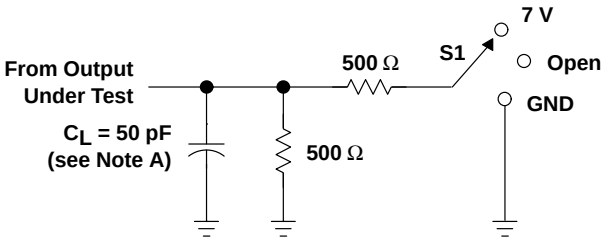
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		V_{CC} = 4 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.25		0.25	ns
t_{pd}	S	A or B	1.6	6.2	1.7	6.6	ns
t_{en}	S	A or B	1.3	6.3	1.9	7.1	ns
	$\overline{OE}$		1.4	6.4	2.3	7.3	
t_{dis}	S	A or B	1.1	7.4	1.9	7.9	ns
	$\overline{OE}$		2.3	7	2.2	7.3	

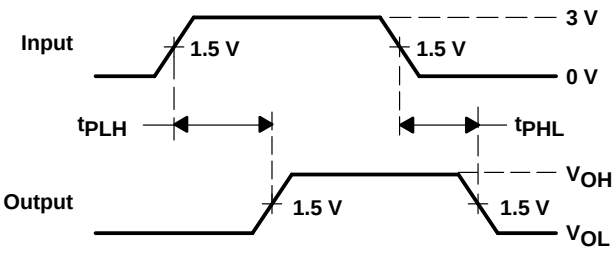
¶ This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

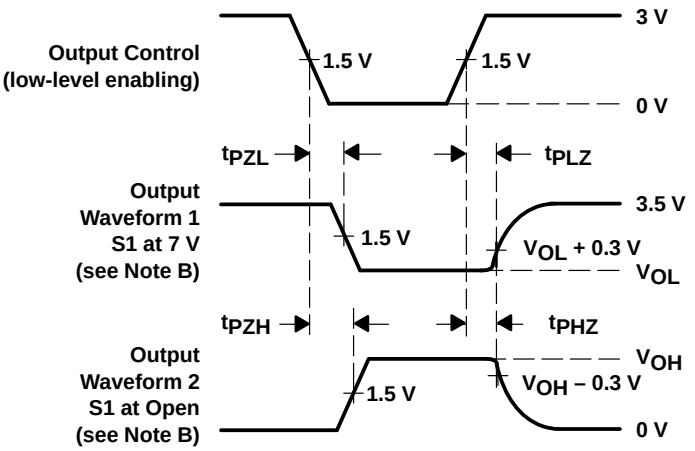


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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