

# SN74CBT3257

## QUADRUPL 2-BIT TO 1-BIT FET MULTIPLEXER/DEMULTIPLEXER

SCDS017F – MAY 1995 – REVISED MAY 1997

- Functionally Equivalent to QS3257
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Quarter-Size Small-Outline (DBQ), and Thin Shrink Small-Outline (PW) Packages

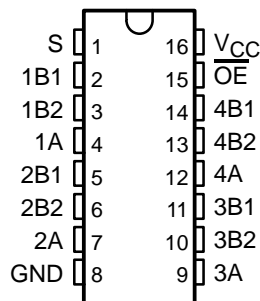
### description

The SN74CBT3257 is a quadruple 2-bit to 1-bit high-speed TTL-compatible FET demultiplexer/multiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

Output-enable ( $\overline{OE}$ ) and select-control (S) select the appropriate B1 and B2 outputs for the A-input data.

The SN74CBT3257 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

D, DB, DBQ, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	A = B1
H	L	A = B2



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**TEXAS  
INSTRUMENTS**

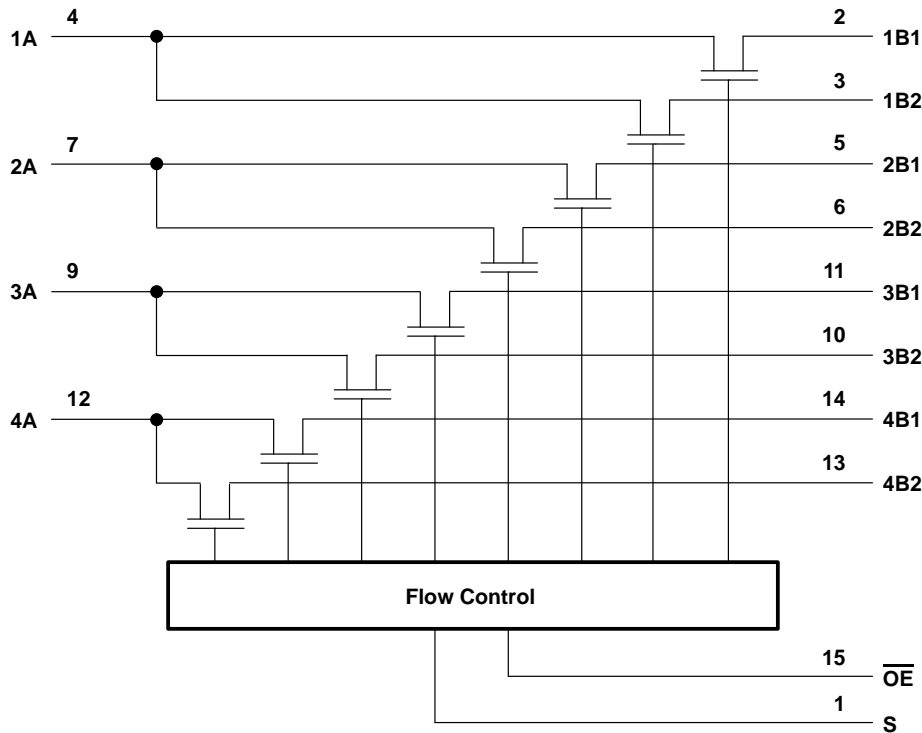
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_K$ ( $V_{I/O} < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	113°C/W
DB package	131°C/W
DBQ package	139°C/W
PW package	149°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4	5.5	V
$V_{IH}$ High-level control input voltage	2		V
$V_{IL}$ Low-level control input voltage		0.8	V
$T_A$ Operating free-air temperature	–40	85	°C

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2	V
$I_I$		$V_{CC} = 5.5\text{ V}$ , $V_I = 5.5\text{ V}$ or GND			$\pm 1$	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND			3	$\mu\text{A}$
$\Delta I_{CC}^\ddagger$	Control pins	$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND			2.5	mA
$C_i$	Control pins	$V_I = 3\text{ V}$ or 0		3.5		pF
$C_{io}(\text{OFF})$	A port	$V_O = 3\text{ V}$ or 0, $\overline{OE} = V_{CC}$		6.5		pF
	B port			4		
$r_{on}^\S$		$V_{CC} = 4\text{ V}$ , $V_I = 2.4\text{ V}$ , $I_I = 15\text{ mA}$		14	20	$\Omega$
		$V_{CC} = 4.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	7
				$I_I = 30\text{ mA}$	5	7
			$V_I = 2.4\text{ V}$ , $I_I = 15\text{ mA}$		10	15

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

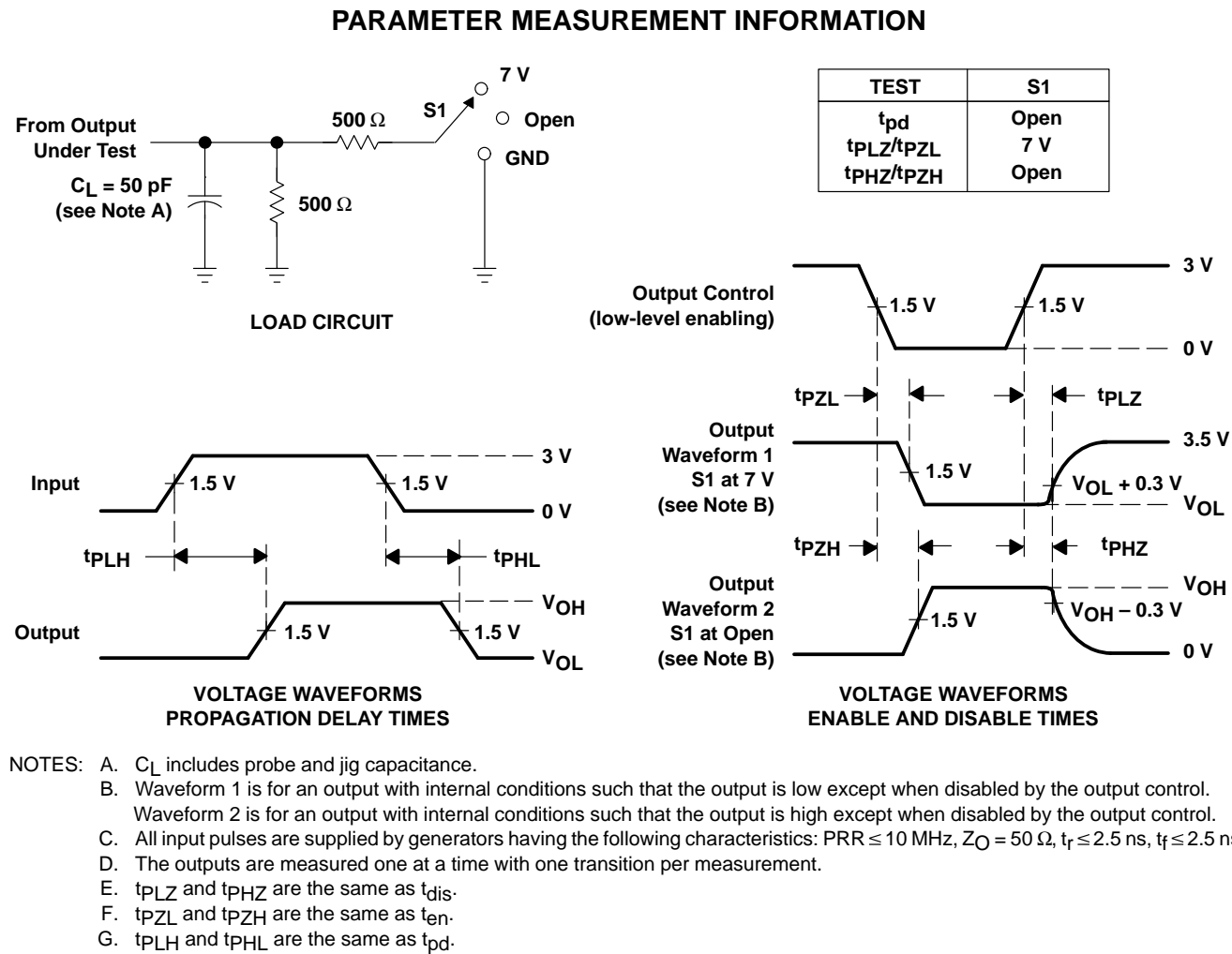
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		$V_{CC} = 4\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^\P$	A or B	B or A		0.25		0.25	ns
$t_{pd}$	S	A or B	1.6	5	5.5		ns
$t_{en}$	S	A or B	1.6	5.2	5.7		ns
	$\overline{OE}$		1.8	5.1	5.6		
$t_{dis}$	S	A or B	1	5	5.2		ns
	$\overline{OE}$		2.2	5.5	5.5		

† This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

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