SCDS009F – MAY 1995 – REVISED AUGUST 1996

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages**

## description

The SN74CBT16232 is a 16-bit to 32-bit synchronous switch used in applications in which two separate datapaths must be multiplexed onto, or demultiplexed from, a single path.

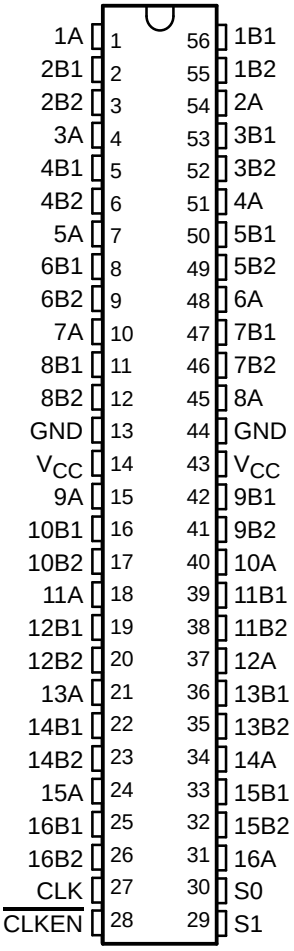
Two select inputs (S0 and S1) control the data flow. A clock (CLK) and a clock enable ($\overline{\text{CLKEN}}$) synchronize the device operation. When $\overline{\text{CLKEN}}$ is high, the bus switch remains in the last clocked function.

The SN74CBT16232 is characterized for operation from –40°C to 85°C.

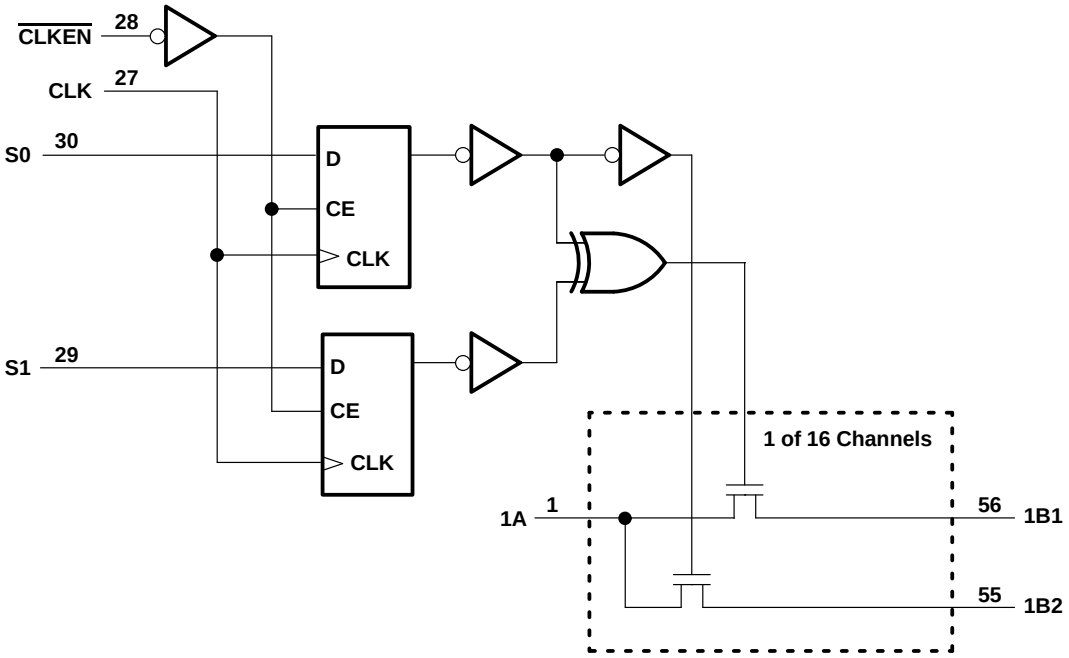
**FUNCTION TABLE**

| S1 | S0 | CLK | $\overline{\text{CLKEN}}$ | FUNCTION |
|---|---|---|---|---|
| X | X | X | H | Last state |
| L | L | ↑ | L | Disconnect |
| L | H | ↑ | L | A = B1 and A = B2 |
| H | L | ↑ | L | A = B1 |
| H | H | ↑ | L | A = B2 |

**DGG OR DL PACKAGE**
**(TOP VIEW)**



## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) . . . . . –50 mA
Maximum power package dissipation at $T_A = 55°C$ (in still air) (see Note 2): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*

## recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | | –1.2 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V or GND | | | | | ±1 | µA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $I_O$ = 0, | $V_I$ = $V_{CC}$ or GND | | | | 3 | µA |
| $\Delta I_{CC}$‡ | Control pins | $V_{CC}$ = 5.5 V, | One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | | 2.5 | mA |
| $C_I$ | Control pins | $V_I$ = 3 V or 0 | | | | | 4.5 | | pF |
| $C_{io(OFF)}$ | A port | $V_O$ = 3 V or 0, | $\overline{CLKEN}$ = 0, | S0 = 0, | S1 = 0 | | 6.5 | | pF |
| | B port | | | | | | 4 | | |
| $r_{on}$§ | | $V_{CC}$ = 4 V, | $V_I$ = 2.4 V, | $I_I$ = 15 mA | | | 14 | 20 | Ω |
| | | $V_{CC}$ = 4.5 V | $V_I$ = 0, | $I_I$ = 64 mA | | | 5 | 7 | |
| | | | $V_I$ = 0, | $I_I$ = 30 mA | | | 5 | 7 | |
| | | | $V_I$ = 2.4 V, | $I_I$ = 15 mA | | | 10 | 15 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

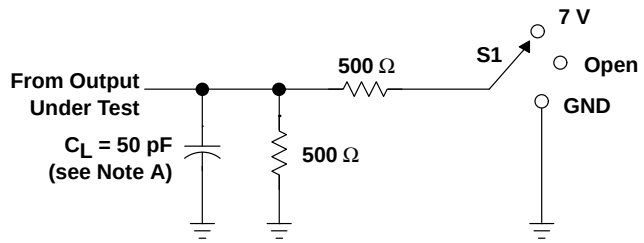
| PARAMETER | | | $V_{CC}$ = 5 V ± 0.5 V | | $V_{CC}$ = 4 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 150 | 0 | 150 | MHz |
| $t_w$ | Pulse duration | CLK high or low | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time | S0, S1 before CLK↑ | 1.9 | | 2.2 | | ns |
| | | $\overline{CLKEN}$ before CLK↑ | 1.9 | | 2.4 | | |
| $t_h$ | Hold time | S0, S1 after CLK↑ | 1 | | 0.5 | | ns |
| | | $\overline{CLKEN}$ after CLK↑ | 1.8 | | 1.9 | | |

## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V ± 0.5 V | | $V_{CC}$ = 4 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 150 | | 150 | | MHz |
| $t_{pd}$¶ | A or B | B or A | | 0.25 | | 0.25 | ns |
| $t_{pd}$ | CLK | A or B | 2 | 5.8 | | 6.1 | ns |
| $t_{en}$ | CLK | A, B1, B2 | 1.8 | 6.2 | | 6.8 | ns |
| $t_{en}$ | CLK | B1 or B2 | 3.1 | 7.9 | | 8.5 | ns |
| $t_{dis}$ | CLK | A or B | 1.9 | 6.2 | | 5.8 | ns |

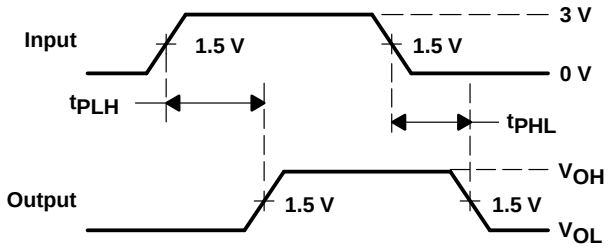
¶ This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

## PARAMETER MEASUREMENT INFORMATION

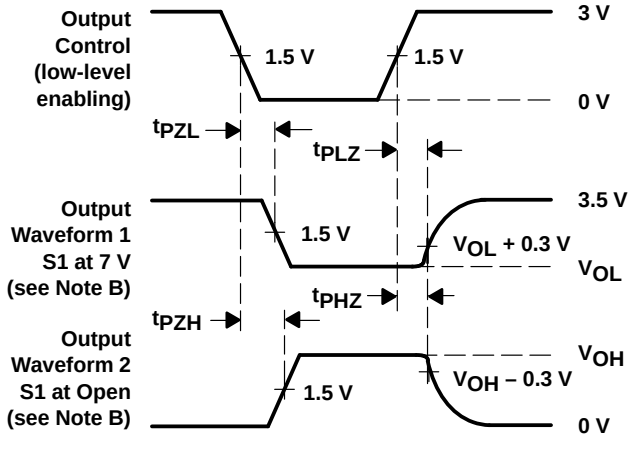



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

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