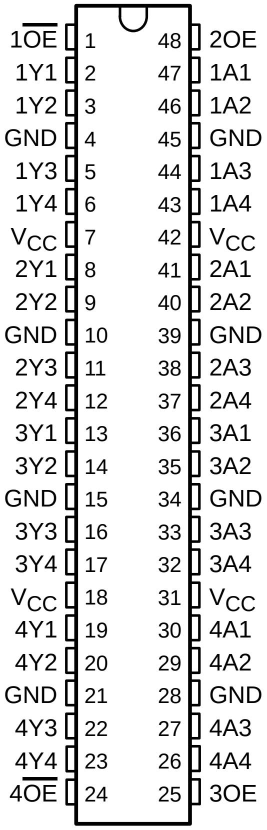
SN54LVTH162241, SN74LVTH162241
3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS692 – MAY 1997

- **Members of the Texas Instruments *Widebus*™ Family**
- **Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **High-Impedance State During Power Up and Power Down**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Power Off Disables Inputs/Outputs, Permitting Live Insertion**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54LVTH162241 . . . WD PACKAGE
SN74LVTH162241 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

These 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. The devices provide noninverting outputs and complementary output-enable (OE and $\overline{OE}$) inputs.

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description (continued)

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

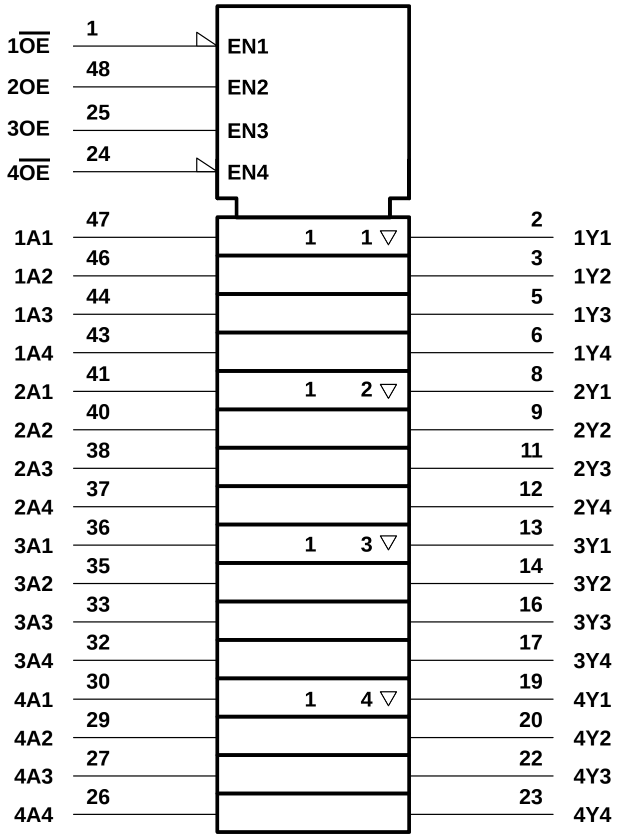
The SN54LVTH162241 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH162241 is characterized for operation from –40°C to 85°C.

FUNCTION TABLES

INPUTS		OUTPUTS
1$\overline{\text{OE}}$, 4$\overline{\text{OE}}$	1A, 4A	1Y, 4Y
L	H	H
L	L	L
H	X	Z

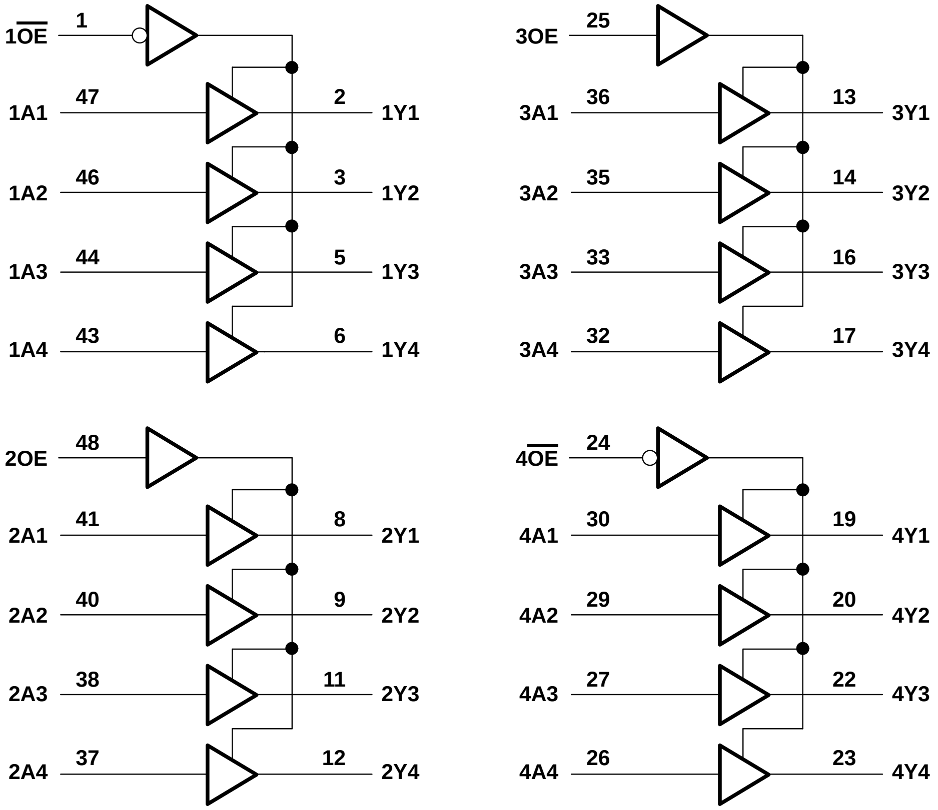
INPUTS		OUTPUTS
2OE, 3OE	2A, 3A	2Y, 3Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O	30 mA
Current into any output in the high state, I_O (see Note 2)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DGV package	93°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVTH162241		SN74LVTH162241		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–12		–12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH162241			SN74LVTH162241			UNIT
				MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 3 V,	I_{OH} = –12 mA	2			2			V
V_{OL}		V_{CC} = 3 V,	I_{OL} = 12 mA			0.8			0.8	V
I_I		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	µA
	Control inputs	V_{CC} = 3.6 V,	$V_I = V_{CC}$ or GND			±1			±1	
	Data inputs	V_{CC} = 3.6 V	$V_I = V_{CC}$			1			1	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			±100			±100	µA
$I_{I(hold)}$	Data inputs	V_{CC} = 3 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	–75			–75			
I_{OZH}		V_{CC} = 3.6 V,	V_O = 3 V			5			5	µA
I_{OZL}		V_{CC} = 3.6 V,	V_O = 0.5 V			–5			–5	µA
I_{OZPU}[‡]		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, OE/$\overline{OE}$ = don’t care				±100			±100	µA
I_{OZPD}[‡]		V_{CC} = 1.5 V to 0, V_O = 0.5 V to 3 V, OE/$\overline{OE}$ = don’t care				±100			±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, $V_I = V_{CC}$ or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}[§]		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0			4			4		pF
C_o		V_O = 3 V or 0			9			9		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This parameter is warranted but not production tested.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

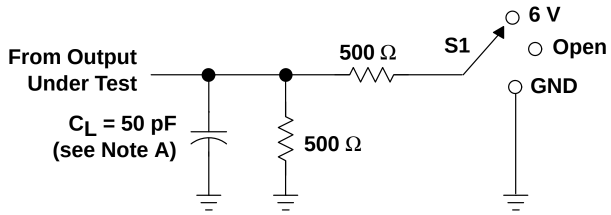
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162241				SN74LVTH162241					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP[†]	MAX	MIN	MAX	
t_{PLH}	A	Y	1.3	4.3		4.9	1.4	3	4.1		4.7	ns
t_{PHL}			1.3	4.3		4.9	1.4	2.4	4.1		4.7	
t_{PZH}	$\overline{OE}$ or OE	Y	1.1	5.2		5.9	1.2	3.5	4.9		5.7	ns
t_{PZL}			1.4	5		5.4	1.5	3.5	4.8		5.2	
t_{PHZ}	$\overline{OE}$ or OE	Y	1.9	5.5		6.2	2	3.7	5.3		5.9	ns
t_{PLZ}			1.9	5.2		5.7	2	3.6	4.9		5.4	
$t_{sk(o)}$[‡]									0.5		0.5	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

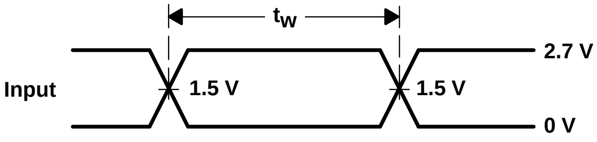
[‡] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

PARAMETER MEASUREMENT INFORMATION

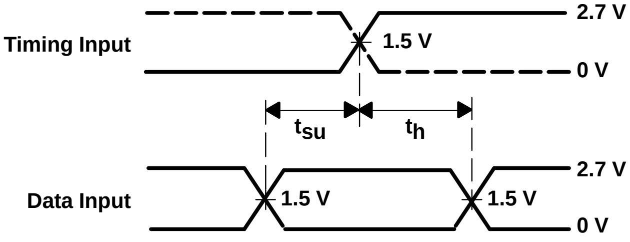


LOAD CIRCUIT

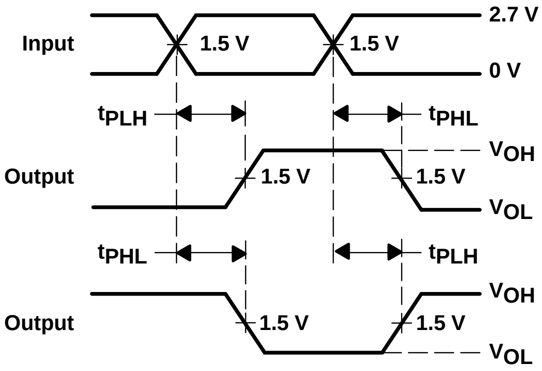
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



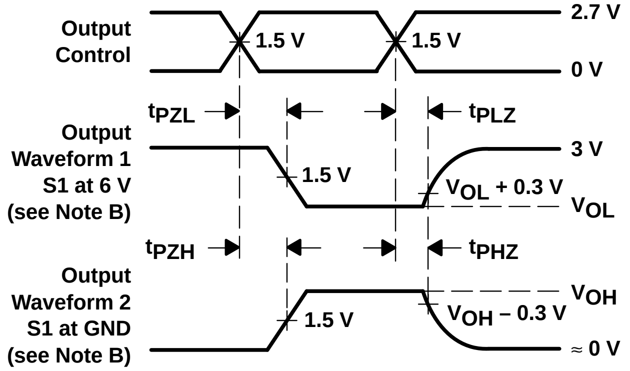
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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