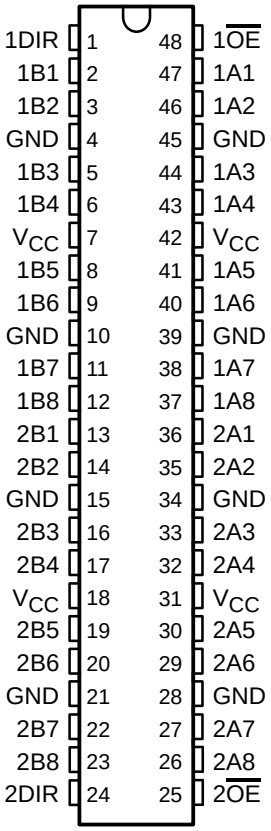
- **Member of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art Advanced Low-Voltage BiCMOS (ALB) Technology Design for 3.3-V Operation**
- **Schottky Diodes on All Inputs to Eliminate Overshoot and Undershoot**
- **Industry Standard ’16245 Pinout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALB16245 is a 16-bit transceiver designed for high-speed, low-voltage (3.3-V) V_{CC} operation. This device is intended to replace the conventional transceiver in any speed-critical path. The small propagation delay is achieved using a unity gain amplifier on the input and feedback resistors from input to output, which allows the output to track the input with a small offset voltage.

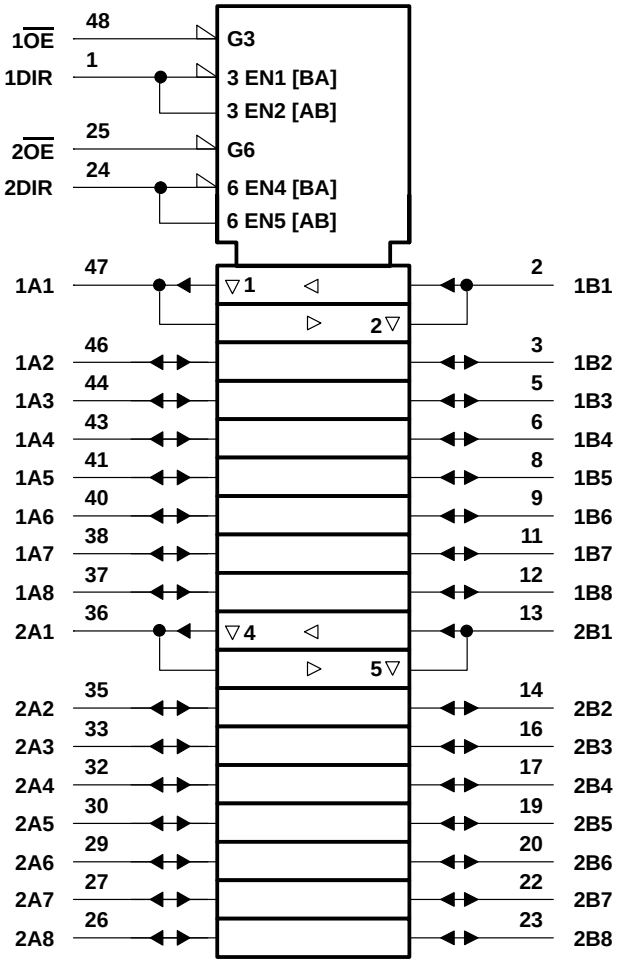
This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The SN74ALB16245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

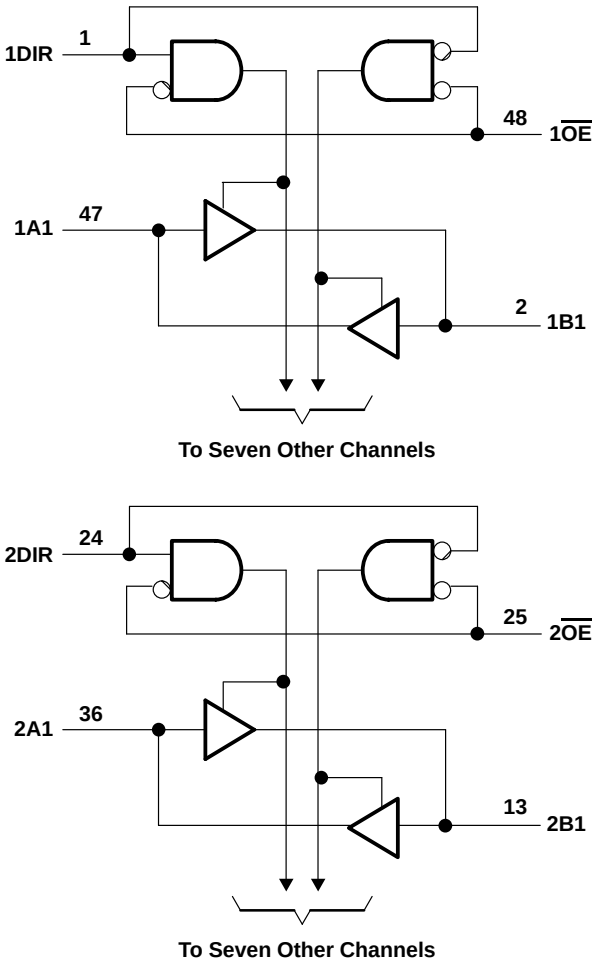
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 89°C/W
DL package . . . . . 94°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
I_{OH}‡	High-level output current			–25	mA
I_{OL}‡	Low-level output current			25	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5	ns/V
T_A	Operating free-air temperature		–40	85	°C

‡ Refer to Figures 1 and 2 for typical I/O ranges.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 3 V	I_I = 18 mA	A or B ports		3.7	V_{CC}+1.2	V
		I_I = –18 mA			–0.9	–1.2	
I_I	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control inputs			±10	µA
		V_I = V_{CC}	A or B ports, $\overline{OE}$ low		0.4	0.6	mA
			A or B ports, $\overline{OE}$ high			25	µA
		V_I = 0	A or B ports, $\overline{OE}$ low		–0.7	–1	mA
			A or B ports, $\overline{OE}$ high			–60	µA
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			0.7	20	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–0.2	–50	µA
I_{CC}/buffer	V_{CC} = 3.6 V,	I_O = ↻,	V_I = V_{CC} or GND		3.7	5.6	mA
I_{CCZ}	V_{CC} = 3.6 V,	Control inputs = V_{CC} or GND				0.8	mA
ΔI_{CC}‡	V_{CC} = 3 V to 3.6 V, One input at V_{CC} –0.6 V, Other inputs at V_{CC} or GND					600	µA
C_i	V_I = 3 V or 0				3.5		pF
C_{io}	V_O = 3 V or 0				7.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

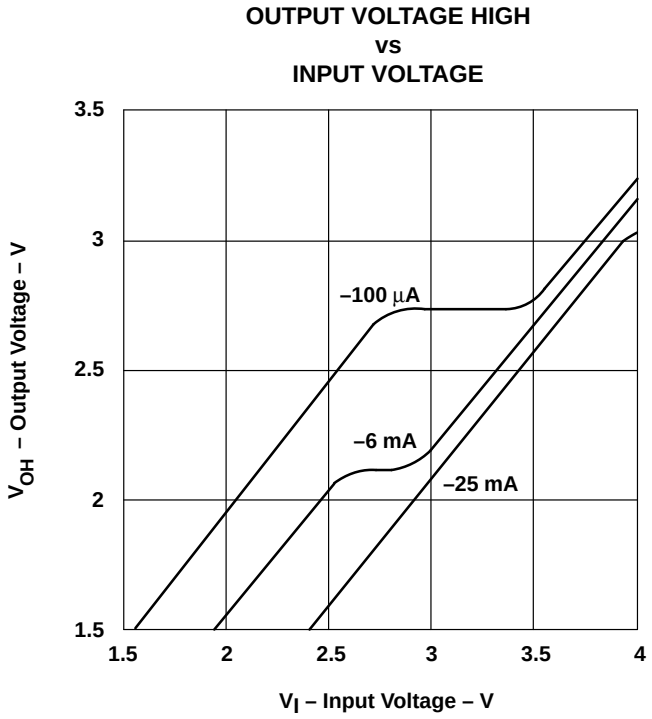


Figure 1. V_{OH} Over Recommended Free-Air Temperature Range

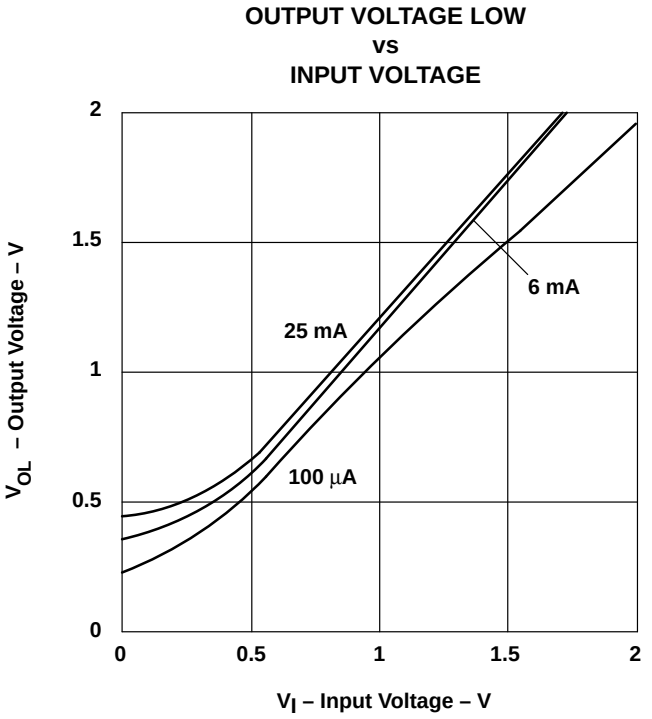


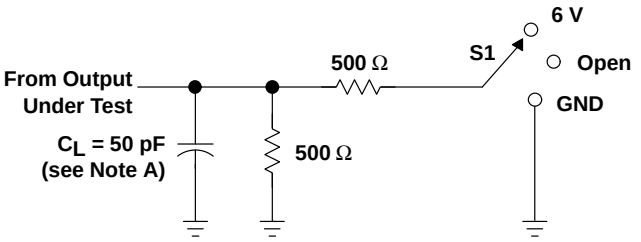
Figure 2. V_{OL} Over Recommended Free-Air Temperature Range

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			UNIT
			MIN	TYP†	MAX	
t_{pd}	A or B	B or A	0.6	1.3	2	ns
t_{en}	$\overline{OE}$	A or B	1.5	3.2	6	ns
t_{dis}	$\overline{OE}$	A or B	1.8	2.8	4.2	ns

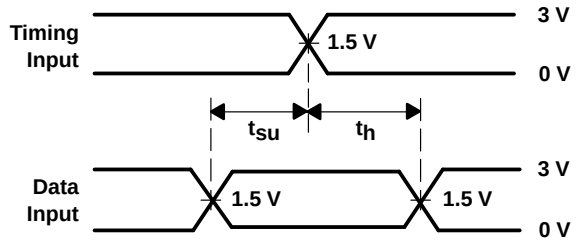
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

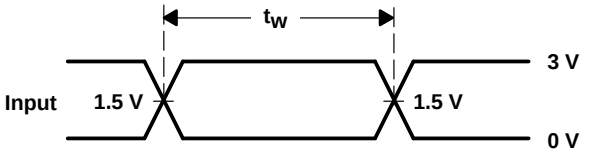


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

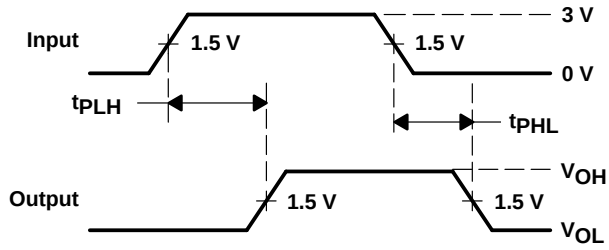
LOAD CIRCUIT



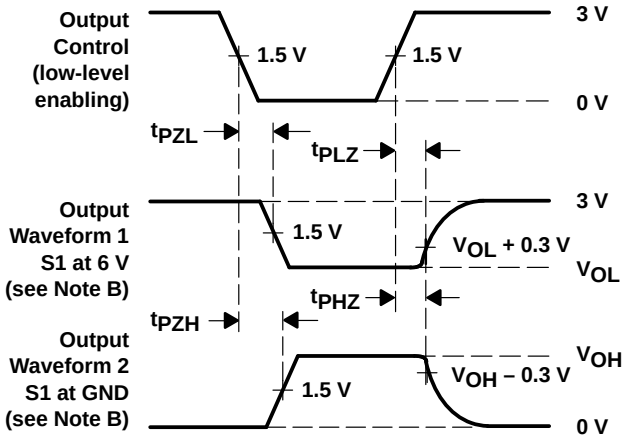
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms

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