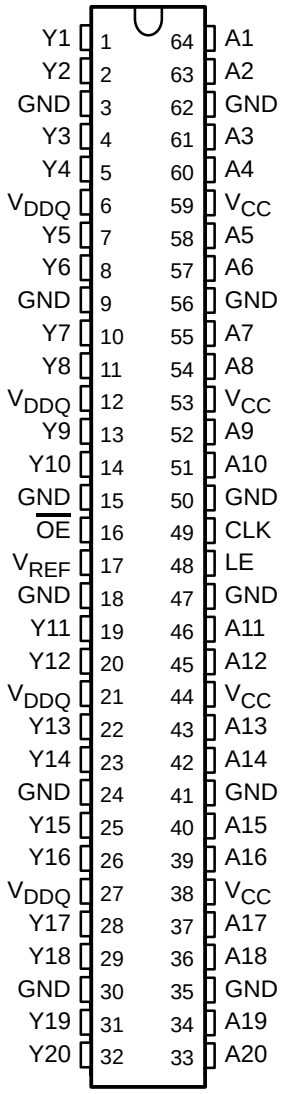
- **Member of the Texas Instruments Widebus™ Family**
- **Supports SSTL_3 Signal Inputs and Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Meets SSTL_3 Class I and Class II Specifications**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Packaged in Plastic Thin Shrink Small-Outline Package**

**DGG PACKAGE**
**(TOP VIEW)**




## description

This 20-bit universal bus driver is designed for 3-V to 3.6-V $V_{CC}$ operation and SSTL_3 or LVTTL I/O levels.

Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when latch enable (LE) is high. The A data is latched if LE is low and clock (CLK) is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74SSTL16837 is characterized for operation from 0°C to 70°C.

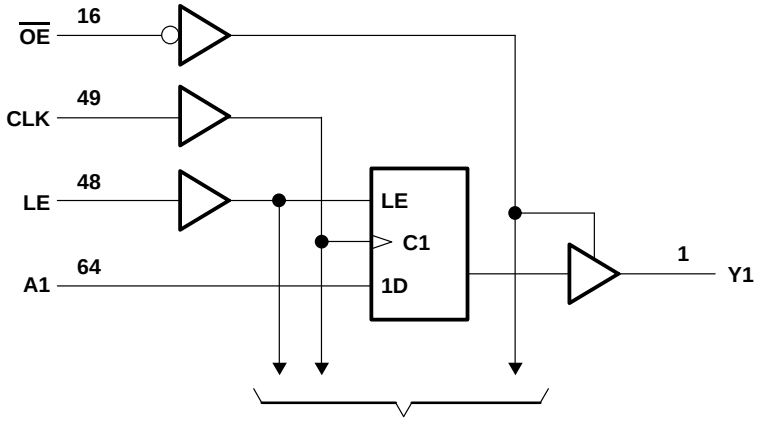
**FUNCTION TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OE}$ | LE | CLK | A | Y |
| L | H | X | H | H |
| L | H | X | L | L |
| L | L | ↑ | H | H |
| L | L | ↑ | L | L |
| L | L | H | X | $Y_0$† |
| L | L | L | X | $Y_0$‡ |
| H | X | X | X | Z |

† Output level before the indicated steady-state input conditions were established, provided that CLK was high before LE went low

‡ Output level before the indicated steady-state input conditions were established

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) . . . . . 73°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O$ > $V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 4)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 3 | | 3.6 | V |
| $V_{DDQ}$ | I/O supply voltage | | 3 | | 3.6 | V |
| $V_{REF}$ | Supply voltage | | 1.3 | 1.5 | 1.7 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage | All pins | $V_{REF}$+200mV | | | V |
| $V_{IL}$ | Low-level input voltage | All pins | | | $V_{REF}$–200mV | V |
| $I_{OH}$ | High-level output current | | | | –20 | mA |
| $I_{OL}$ | Low-level output current | | | | 20 | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $I_I$ = –18 mA | | 3 V | | | –1.2 | V |
| $V_{OH}$ | | $I_{OH}$ = –100 μA | | 3 V to 3.6 V | $V_{CC}$–0.2 | | | V |
| | | $I_{OH}$ = –16 mA | | 3 V | 2.2 | | | |
| | | $I_{OH}$ = –20 mA | | 3 V | 2.1 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA | | 3 V to 3.6 V | | | 0.2 | V |
| | | $I_{OH}$ = 16 mA | | 3 V | | | 0.5 | |
| | | $I_{OH}$ = 20 mA | | 3 V | | | 0.55 | |
| $I_I$ | LE | $V_I$ = 2.1 V or 0.9 V, | $V_{REF}$ = 1.3 V or 1.7 V | 3.6 V | | | ±40 | μA |
| | | $V_I$ = 3.6 V or 0, | $V_{REF}$ = 1.3 V or 1.7 V | 3.6 V | | | ±1.2 | mA |
| | Data inputs, $\overline{OE}$ | $V_I$ = 2.1 V or 0.9 V, | $V_{REF}$ = 1.3 V or 1.7 V | 3.6 V | | | ±5 | μA |
| | | $V_I$ = 3.6 V or 0, | $V_{REF}$ = 1.3 V or 1.7 V | 3.6 V | | | ±5 | |
| | CLK | $V_I$ = 2.1 V or 0.9 V, | $V_{REF}$ = 1.3 V or 1.7 V | 3.6 V | | | ±150 | |
| | | $V_I$ = 3.6 V or 0, | $V_{REF}$ = 1.3 V or 1.7 V | 3.6 V | | | ±4 | mA |
| | $V_{REF}$ | $V_{REF}$ = 1.3 V or 1.7 V | | 3.6 V | | | ±150 | μA |
| $I_{OZ}$ | | $V_O$ = 0.9 V or 2.1 V | | 3.6 V | | | ±10 | μA |
| | | $V_O$ = 0 or 3.6 V | | 3.6 V | | | ±10 | |
| $I_{CC}$ | | $V_I$ = 2.1 V or 0.9 V, | $I_O$ = 0 | 3.6 V | | | 90 | mA |
| | | $V_I$ = 3.6 V or 0, | $I_O$ = 0 | 3.6 V | | | 90 | |
| $C_i$ | Control pin | $V_I$ = 2.1 V or 0.9 V | | 3.3 V | | 2.5 | | pF |
| | A port | | | | | 2 | | |
| $C_o$ | Y port | $V_O$ = 2.1 V or 0.9 V | | 3.3 V | | 3 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | | 200 | MHz |
| $t_w$ | Pulse duration | LE high | | 2.5 | | ns |
| | | CLK high or low | | 2.5 | | |
| $t_{su}$ | Setup time | A before CLK↑ | LE low | 1.5 | | ns |
| | | A before LE↓ | CLK high | 1.5 | | |
| | | | CLK low | 2 | | |
| $t_h$ | Hold time | A after CLK↑ | LE low | 1 | | ns |
| | | A after LE↓ | | 1 | | |

**switching characteristics over recommended operating free-air temperature range, Class I, $V_{REF} = V_{TT} = V_{CC} \times 0.45$ and $C_L$ = 10 pF (unless otherwise noted) (see Figure 1)**

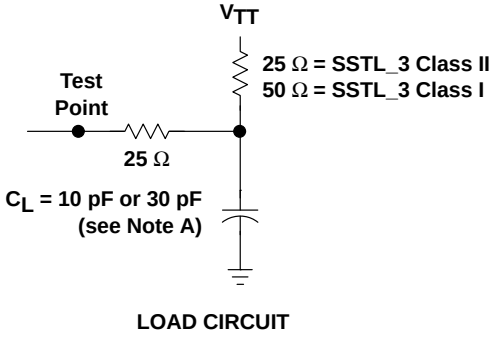
| PARAMETER† | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $f_{max}$ | | | 200 | | MHz |
| $t_{pd}$ | A | Y | 1.1 | 4 | ns |
| | LE | | 1.5 | 4.1 | |
| | CLK | | 1 | 3 | |
| $t_{en}$ | $\overline{OE}$ | Y | 1.8 | 5.5 | ns |
| $t_{dis}$ | $\overline{OE}$ | Y | 1.8 | 6 | ns |

† These parameters are warranted but not production tested.

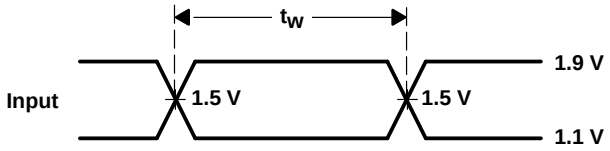
**switching characteristics over recommended operating free-air temperature range, Class II, $V_{REF} = V_{TT} = V_{CC} \times 0.45$ and $C_L$ = 30 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $f_{max}$ | | | 200 | | MHz |
| $t_{pd}$ | A | Y | 1.1 | 4.2 | ns |
| | LE | | 1.5 | 4.3 | |
| | CLK | | 1 | 3.2 | |
| $t_{en}$ | $\overline{OE}$ | Y | 1.8 | 5.5 | ns |
| $t_{dis}$ | $\overline{OE}$ | Y | 1.8 | 6 | ns |

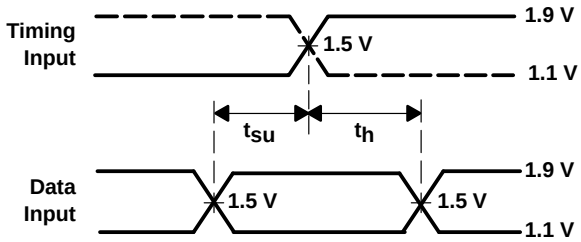
## PARAMETER MEASUREMENT INFORMATION



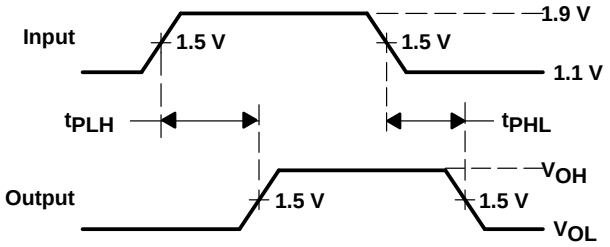

LOAD CIRCUIT



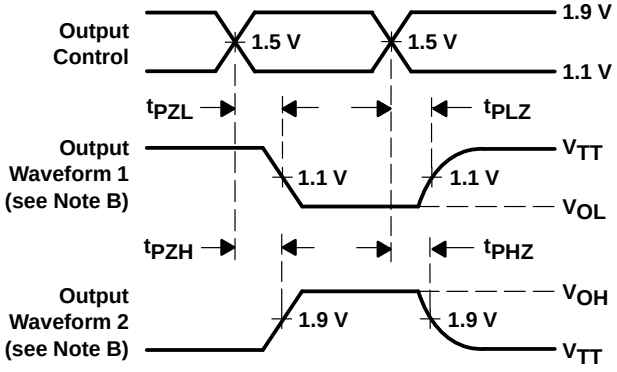

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 1 ns, $t_f$ ≤ 1 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $V_{REF} = V_{TT} = V_{CC} \times 0.45$
F. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
G. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
H. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

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