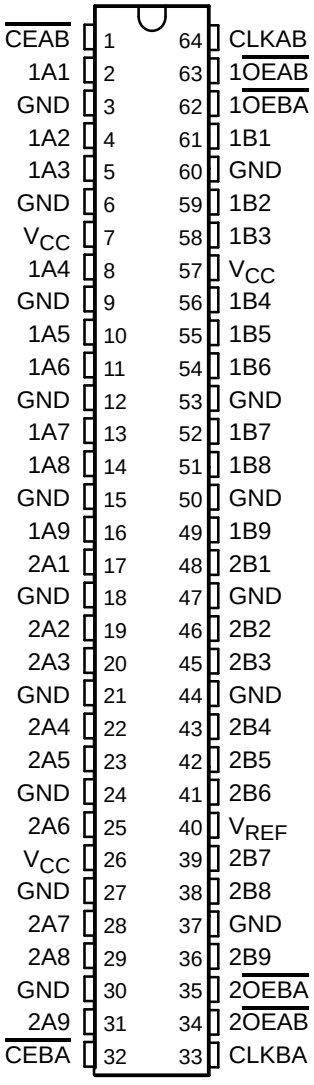
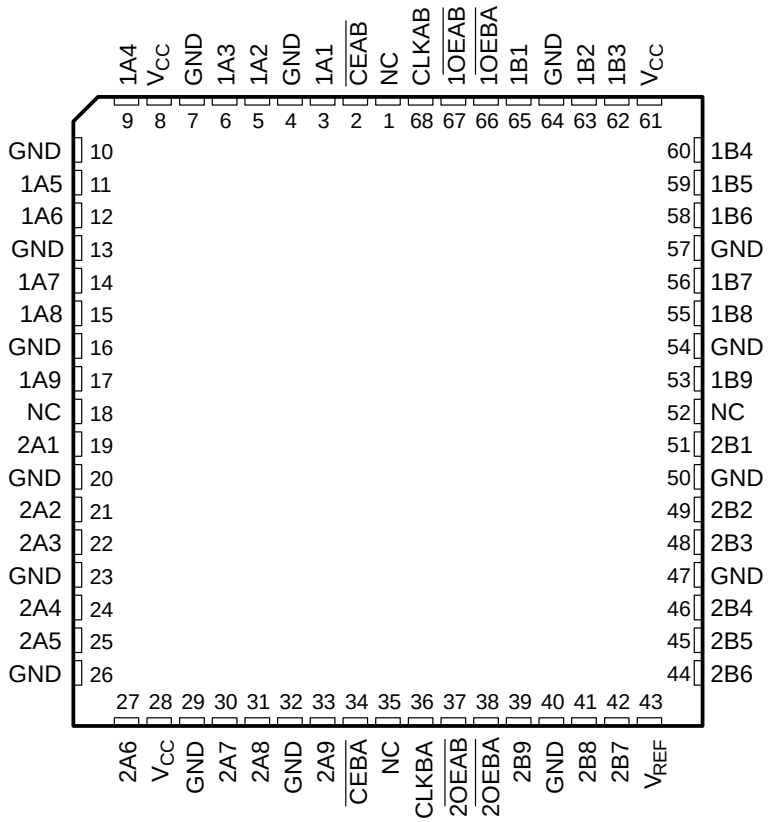
- **Members of the Texas Instruments *Widebus*™ Family**
- **Translate Between GTL/GTL+ Signal Levels and LVTTL or 5-V TTL Signal Levels**
- **Support Mixed-Mode (3.3 V and 5 V) Signal Operation on A Port and Control Inputs**
- **Support GTL/GTL+ Signal Operation on B Port**
- **D-Type Flip-Flops With Qualified Storage Enable**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port**
- **Flow-Through Architecture Facilitates Printed Circuit Board Layout**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Ceramic Quad Flat (HV) Packages**

SN74GTL16923 . . . DGG PACKAGE
(TOP VIEW)



SN54GTL16923 . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection

ADVANCE INFORMATION

description

These 18-bit registered bus transceivers contain two sets of D-type flip-flops for temporary storage of data flowing in either direction.

The B port operates at GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) and GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) levels, while the A port and control pins are compatible with LVTTL and 5-V TTL logic levels.

Data flow in each direction is controlled by the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and the clock (CLKAB and CLKBA) inputs. The clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs are used to enable or disable the clock for all 18 bits at a time. However, $\overline{OEAB}$ and $\overline{OEBA}$ are designed to control each 9-bit transceiver independently, which makes the device more versatile.

For A-to-B data flow, the device operates on the low-to-high transition of CLKAB if $\overline{CEAB}$ is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, CLKBA, and $\overline{CEBA}$.

Active bus-hold circuitry is provided to hold unused or floating TTL inputs at a valid logic state.

V_{REF} is the reference voltage input for the GTL B port.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54GTL16923 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74GTL16923 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

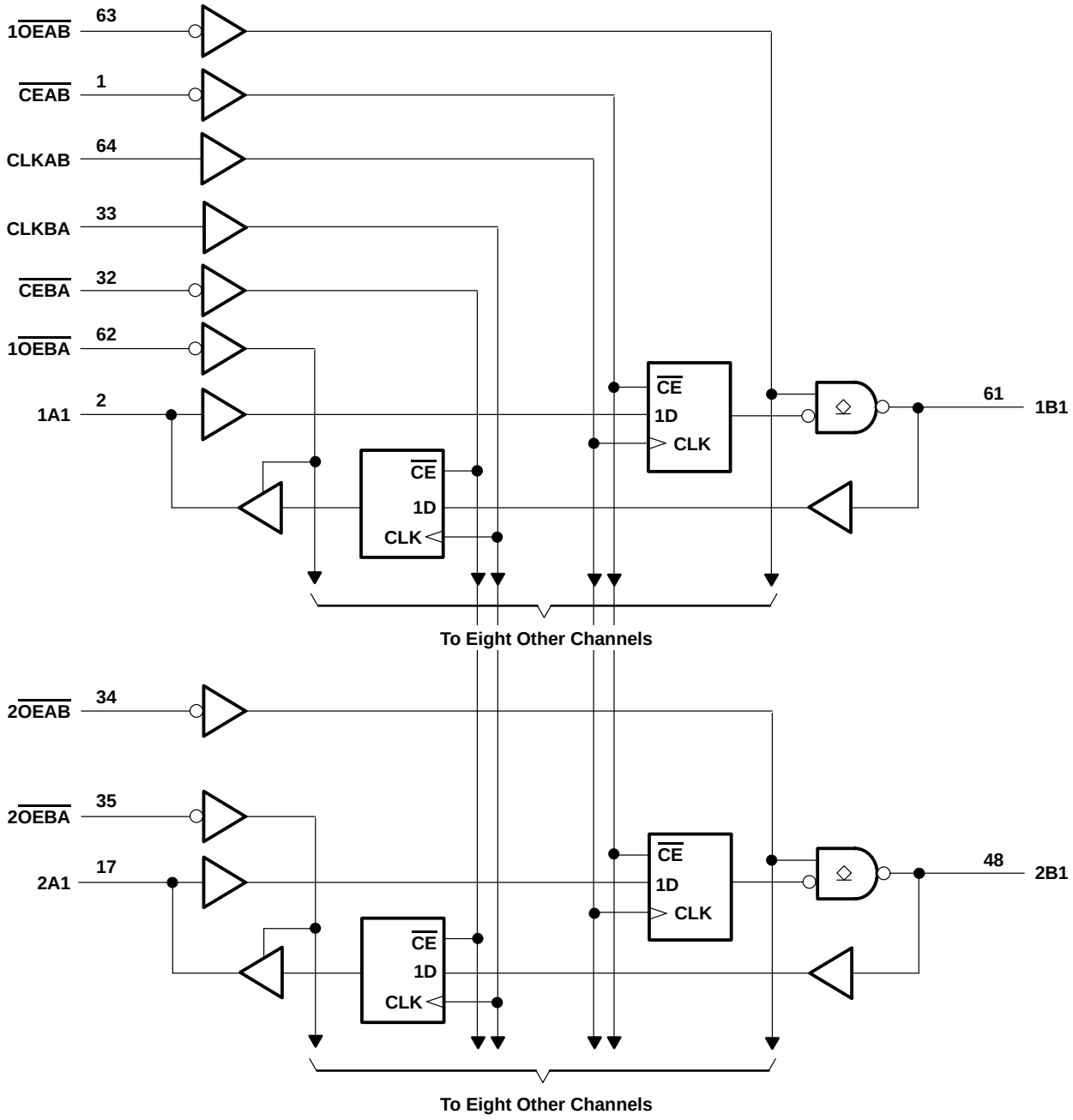
INPUTS				OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	CLKAB	A		
X	H	X	X	Z	
H	L	X	X	B_0‡	Latched storage of A data
X	L	H or L	X	B_0‡	
L	L	↑	L	L	Clocked storage of A data
L	L	↑	H	H	

† A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, CLKBA, and $\overline{CEBA}$.

‡ Output level before the indicated steady-state input conditions are established

ADVANCE INFORMATION

logic diagram (positive logic)



Pin numbers shown are for the DGG package.

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: 3.3 V . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A port . . . . . –0.5 V to 7 V
B port . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1): A port . . . –0.5 V to 7 V
B port . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . . 48 mA
B port . . . . . 100 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 73°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

ADVANCE INFORMATION

recommended operating conditions (see Note 3)

			SN54GTL16923			SN74GTL16923			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3.15	3.3	3.45	3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	1.35	1.5	1.65	
V_{REF}	Supply voltage	GTL	0.74	0.8	0.87	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}			V_{TT}	V
		Except B port			5.5			5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+50 mV			V_{REF}+50 mV			V
		Except B port	2			2			
V_{IL}	Low-level input voltage	B port			V_{REF}–50 mV			V_{REF}–50 mV	V
		Except B port			0.8			0.8	
I_{IK}	Input clamp current				–18			–18	mA
I_{OH}	High-level output current	A port			–24			–24	mA
I_{OL}	Low-level output current	A port			24			24	mA
		B port			50			50	
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range for GTL/GTL+ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54GTL16923			SN74GTL16923			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	A port	V_{CC} = MIN to MAX‡,	I_{OH} = –100 μA	V_{CC}–0.2			V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			2.4			
			I_{OH} = –24 mA	2			2			
V_{OL}	A port	V_{CC} = MIN to MAX‡,	I_{OL} = 100 μA			0.2			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4			0.4	
			I_{OL} = 24 mA			0.5			0.5	
	B port	V_{CC} = MIN to MAX‡,	I_{OL} = 100 μA			0.2			0.2	
		V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2			0.2	
			I_{OL} = 40 mA			0.4			0.4	
			I_{OL} = 50 mA			0.55			0.55	
I_I	B port	V_{CC} = 3.45 V,	V_I = V_{TT} or GND			±5			±5	μA
	A port and control inputs	V_{CC} = 3.45 V,	V_I = 5.5 V or GND			±20			±20	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			100			100	μA
$I_{I(hold)}$	A port	V_{CC} = 3.15 V	V_I = 0.8 V	75			75			μA
			V_I = 2 V	–75			–75			
		V_{CC} = 3.45 V§,	V_I = 0.8 V to 2 V			±500			±500	
I_{OZ}¶	A port	V_{CC} = 3.45 V,	V_O = V_{CC} or GND			±10			±10	μA
I_{OZH}	B port	V_{CC} = 3.45 V,	V_O = 1.5 V			10			10	μA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I = V_{CC} or GND	Outputs high					24		mA
			Outputs low					27		
			Outputs disabled					27		
ΔI_{CC}#		V_{CC} = 3.45 V, A port or control inputs at V_{CC} or GND, One input at V_{CC} – 0.6 V				1			1	mA
C_i	Control inputs	V_I = 3.15 V or 0								pF
C_{io}	A port	V_O = 3.15 V or 0								pF
	B port	Per IEEE 1194.1								

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
¶ For I/O ports, the parameter I_{OZ} includes the input leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature for GTL (unless otherwise noted)†

			SN54GTL16923		SN74GTL16923		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	200	0	200	MHz
t_w	Pulse duration, CLK high or low						ns
t_{su}	Setup time	Data before CLK↑					ns
		$\overline{CE}$ before CLK↑					
t_h	Hold time	Data after CLK↑					ns
		$\overline{CE}$ after CLK↑					

† These parameters are warranted but not production tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature for GTL (see Figure 1)†

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16923			SN74GTL16923			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}			200			200			MHz
t_{PLH}	CLKAB	B							ns
t_{PHL}									
t_{PLH}	$\overline{OEAB}$	B							ns
t_{PHL}									
Slew rate	Both transitions								V/ns
t_r	Transition time, B outputs (0.6 V to 1 V)								ns
t_f	Transition time, B outputs (1 V to 0.6 V)								ns
t_{PLH}	CLKBA	A							ns
t_{PHL}									
t_{en}	$\overline{OEBA}$	A							ns
t_{dis}									

† These parameters are warranted but not production tested.
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature for GTL+ (unless otherwise noted)

			SN54GTL16923		SN74GTL16923		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	200	0	200	MHz
t_w	Pulse duration, CLK high or low				2		ns
t_{su}	Setup time	Data before CLK↑			2		ns
		$\overline{CE}$ before CLK↑			3		
t_h	Hold time	Data after CLK↑			0		ns
		$\overline{CE}$ after CLK↑			0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature for GTL+ (see Figure 1)

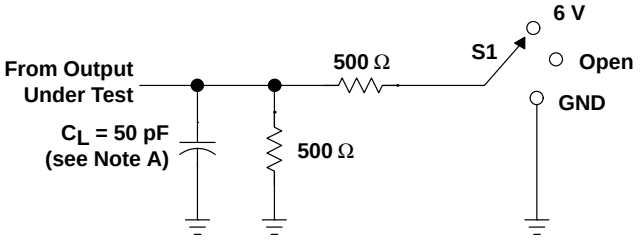
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16923			SN74GTL16923			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			200			200			MHz
t_{PLH}	CLKAB	B						5.5	ns
t_{PHL}								5.5	
t_{PLH}	$\overline{OEAB}$	B						5	ns
t_{PHL}								5	
Slew rate	Both transitions					0.3		0.8	V/ns
t_r	Transition time, B outputs (0.6 V to 1.3 V)					0.9		2.3	ns
t_f	Transition time, B outputs (1.3 V to 0.6 V)					0.9		2.3	ns
t_{PLH}	CLKBA	A						5.5	ns
t_{PHL}								5.5	
t_{en}	$\overline{OEBA}$	A						6.5	ns
t_{dis}								6	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

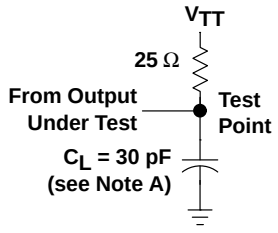
ADVANCE INFORMATION

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION
V_{TT} = 1.5 V, V_{REF} = 1 V

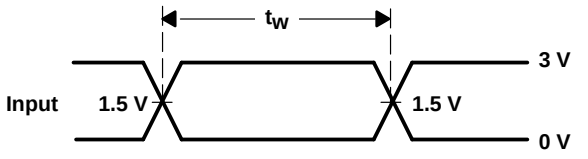


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

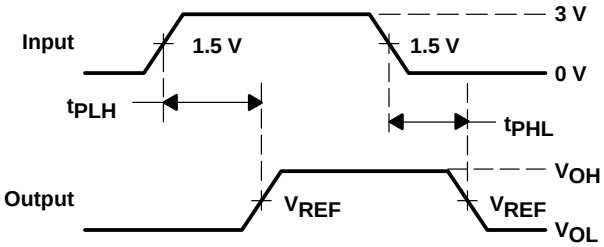


LOAD CIRCUIT FOR A OUTPUTS

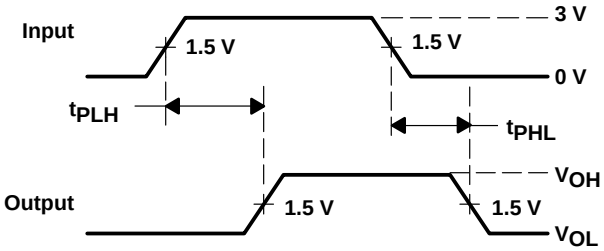
LOAD CIRCUIT FOR B OUTPUTS



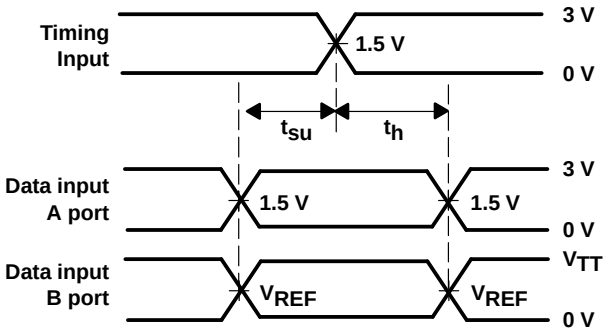
VOLTAGE WAVEFORMS
PULSE DURATION



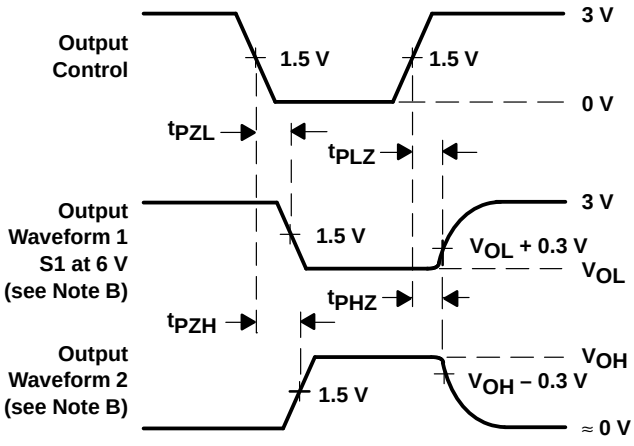
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLKAB to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLKBA to A port)



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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