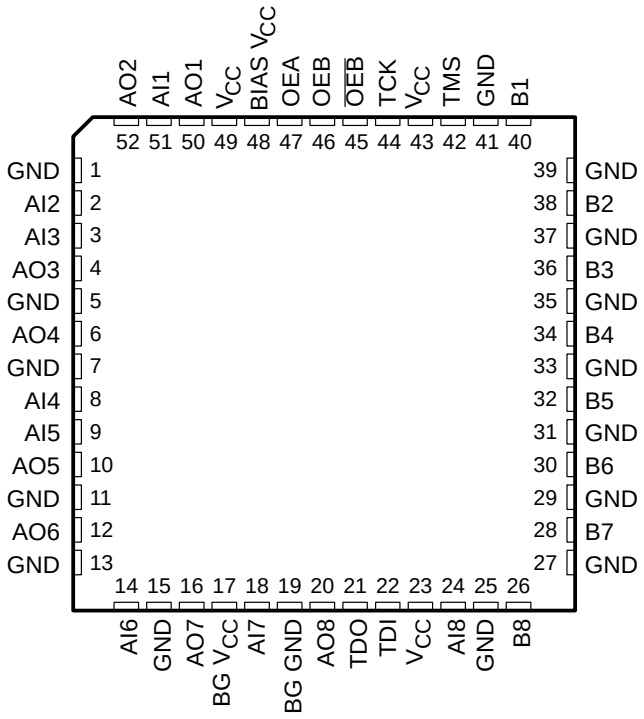
- **Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards**
- **TTL A Port, Backplane Transceiver Logic B Port**
- **Open-Collector B-Port Outputs Sink 100 mA**
- **Minimum B-Port Edge Rate = 2 ns**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **Packaged in Plastic Quad-Flat Packages (RC) With 0.65-mm Pin Pitches**
- **B-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**

RC PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The SN74FB2042 is an 8-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments. It is specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The B port operates at BTL-signal levels. The open-collector B ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and $\overline{\text{OEB}}$, are provided for the B outputs. When OEB is high and $\overline{\text{OEB}}$ is low, the B port is active and reflects the data present at the A-input pins. When OEB is low, $\overline{\text{OEB}}$ is high, or V_{CC} is typically less than 2.5 V, the B port is turned off.

The A port operates at TTL-signal levels and has split input and output pins. The A outputs reflect the data at the B port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the SN74FB2042. Currently TMS and TCK are not connected and TDI is shorted to TDO.

description (continued)

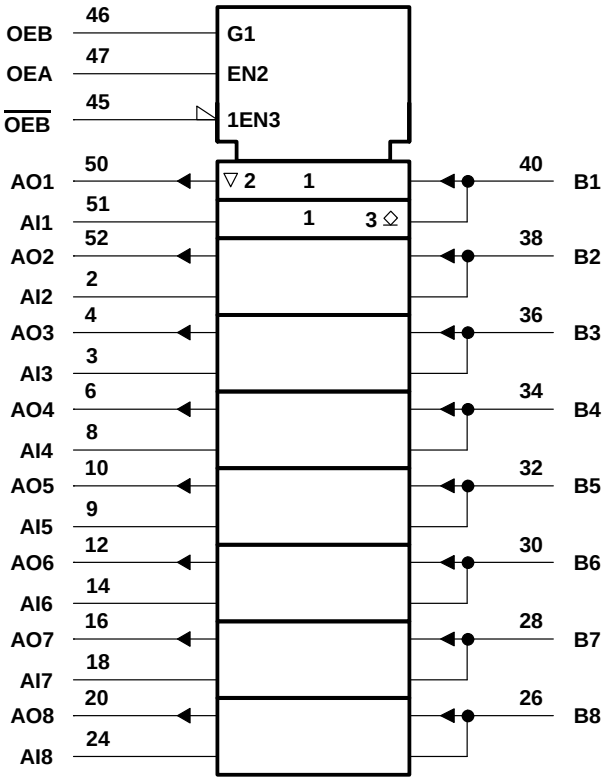
BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN74FB2042 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			FUNCTION
OEB	$\overline{OEB}$	OEA	
L	X	L	Isolation
X	H	L	
L	X	H	B data to AO bus
X	H	H	
H	L	L	AI data to B bus
H	L	H	AI data to B bus, B data to AO bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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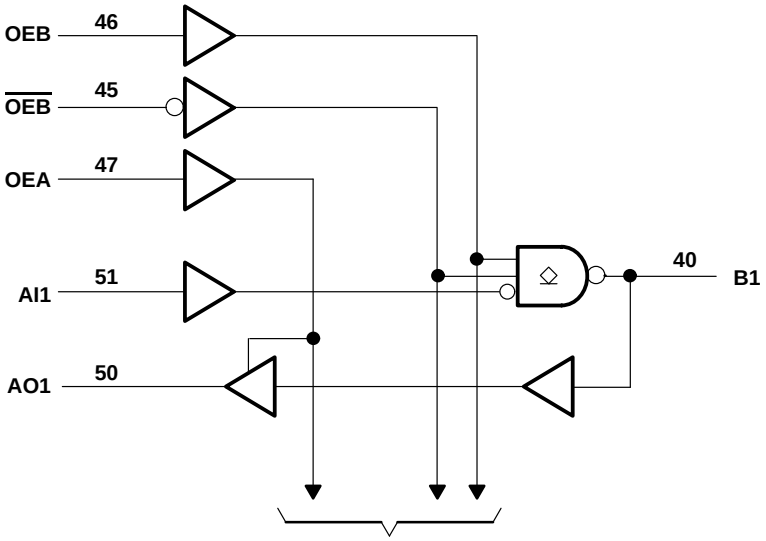
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range: (except B port) . . . . . –1.2 V to 7 V
(B port) . . . . . –1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) . . . . . –40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state . . . . . –0.5 V to V_{CC}
Current applied to any single output in the low state: (AO port) . . . . . 48 mA
(B port) . . . . . 200 mA
Maximum power dissipation at T_A = 55°C (in still air): RC package . . . . . 1.4 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	B port	1.62		2.3	V
		Except B port	2			
V_{IL}	Low-level input voltage	B port	0.75		1.47	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO port			–3	mA
I_{OL}	Low-level output current	AO port			24	mA
		B port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	B port	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
	Except B port	V_{CC} = 4.5 V,	I_I = –40 mA			–0.5	V
V_{OH}	AO port	V_{CC} = 4.5 V	I_{OH} = –1 mA				V
			I_{OH} = –3 mA	2.5	3.3		
V_{OL}	AO port	V_{CC} = 4.5 V	I_{OL} = 20 mA				V
			I_{OL} = 24 mA		0.35	0.5	
	B port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA			1.15	
I_I	Except B port	V_{CC} = 5.5 V,	V_I = 5.5 V			50	µA
I_{IH}‡	Except B port	V_{CC} = 5.5 V,	V_I = 2.7 V			50	µA
I_{IL}‡	Except B port	V_{CC} = 5.5 V	V_I = 0.5 V			–50	µA
	B port†		V_I = 0.75 V			–100	
I_{OH}	B port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100	µA
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			–50	µA
I_{OS}§	AO port	V_{CC} = 5.5 V,	V_O = 0	– 30		–150	mA
I_{CC}	AI port to B port	V_{CC} = 5.5 V,	I_O = 0		25		mA
	B port to AO port				60		
	Outputs disabled						
C_i	AI port and control inputs	V_I = V_{CC} or GND					pF
C_o	AO port	V_O = V_{CC} or GND					pF
C_{io}	B port per P1194.0	V_{CC} = 0 to 4.5 V				6	pF
		V_{CC} = 4.5 V to 5.5 V				5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	AI	B		4				ns
t_{PHL}				3.5				
t_{PLH}	B	AO		3.7				ns
t_{PHL}				3.8				
t_{PLH}	OEB	B		4.7				ns
t_{PHL}				3.9				
t_{PLH}	$\overline{OEB}$	B		4.5				ns
t_{PHL}				3.8				
t_{PZH}	OEA	AO		3.2				ns
t_{PZL}				3				
t_{PHZ}	OEA	AO		3				ns
t_{PLZ}				2.7				
$t_{sk(p)}$	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	AI to B or B to AO					0.75	ns
$t_{sk(o)}$	Skew between drivers in the same package	AI to B or B to AO		1	1.5		2	ns
t_t	Transition time, B outputs (1.3 V to 1.8 V)			2		1	3	ns
t_{PR}	B-port input pulse rejection					1		ns

live insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V,	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V			450	µA
		V_{CC} = 4.5 to 5.5 V,				10	
V_O	B port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62		2.1	V
I_O	B port	V_{CC} = 0 ,	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1			µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V			100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100	

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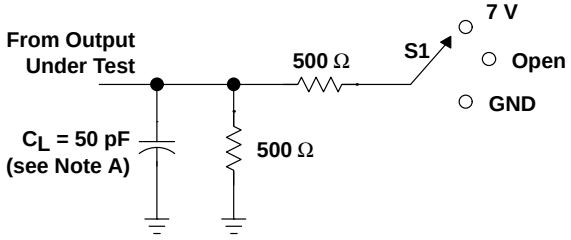
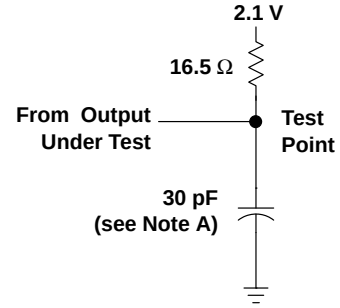
PARAMETER MEASUREMENT INFORMATION

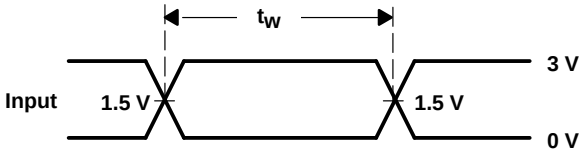


LOAD CIRCUIT FOR A OUTPUTS

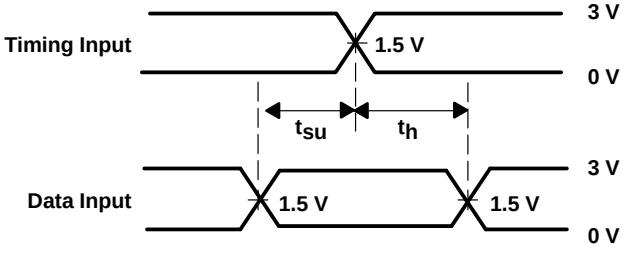


LOAD CIRCUIT FOR B OUTPUTS

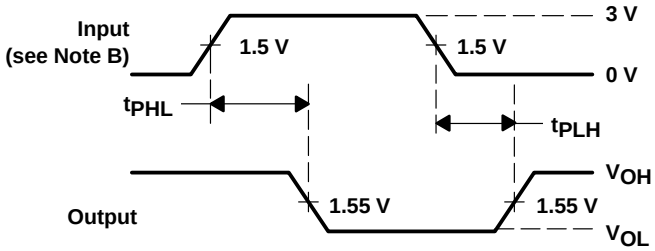
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



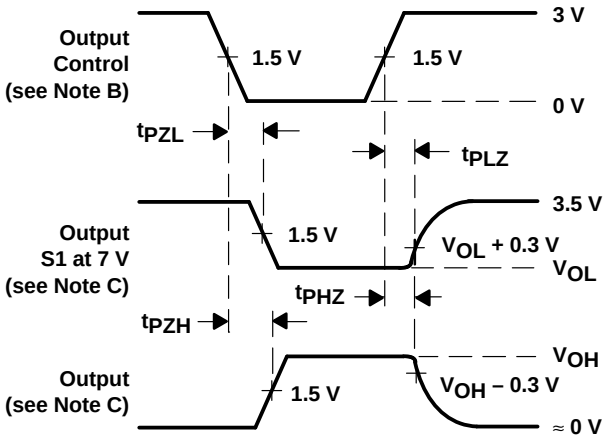
VOLTAGE WAVEFORMS
PULSE DURATION



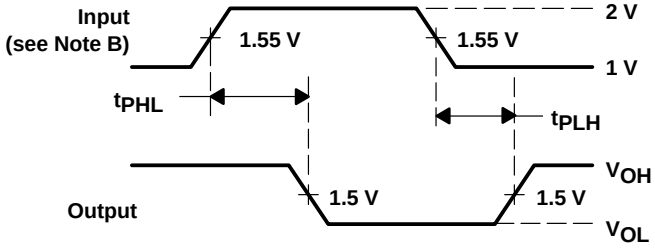
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL Inputs - PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL Inputs - PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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