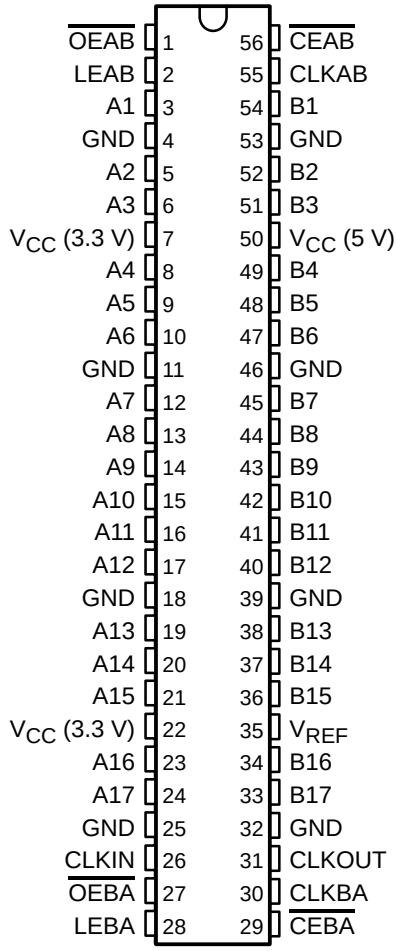
- **Translate Between GTL Signal Levels and LVTTL or 5-V TTL Signal Levels**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Support Mixed-Mode Signal Operation on A Port**
- **Universal Bus Transceiver (*UBT*™) Combines D-Type Latches and D-Type Flip-Flops With Qualified Storage Enable**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port**
- **Flow-Through Architecture Facilitates Printed-Circuit-Board Layout**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Ceramic Flat (WD) Packages**

SN54GTL16616 . . . WD PACKAGE
SN74GTL16616 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 17-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. The ’GTL16616 provide for a copy of CLKAB at GTL logic levels (CLKOUT) and also provide a conversion of the GTL clock to a TTL environment (CLKIN).

The B port operates at GTL levels while the A port and control inputs are compatible with LVCMOS, LVTTL, or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTL16616 is available in TI’s shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

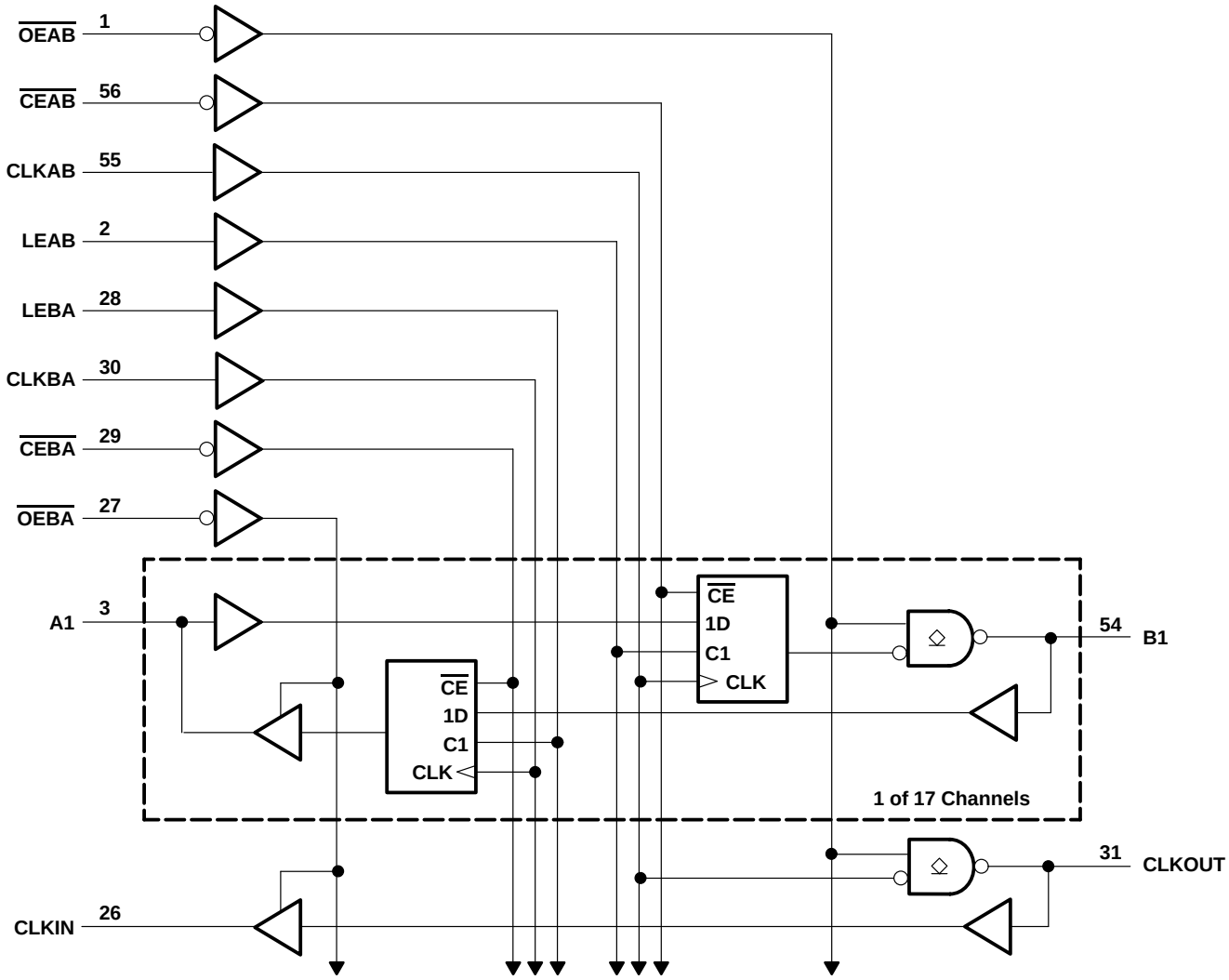
The SN54GTL16616 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74GTL16616 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H or L	X	B_0‡	
L	L	L	H or L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown: B-to-A data flow is similar, but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CEBA}$.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
§ Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: 3.3 V . . . . . –0.5 V to 4.6 V
5 V . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1): A port . . . . . –0.5 V to 7 V
B port . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1): A port . . . –0.5 V to 7 V
B port . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . . 128 mA
B port . . . . . 80 mA
Current into any A-port output in the high state, I_O (see Note 2) . . . . . 64 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			SN54GTL16616			SN74GTL16616			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	3.3 V	3.15	3.3	3.45	3.15	3.3	3.45	V
		5 V	4.75	5	5.25	4.75	5	5.25	
V_{REF}	Supply voltage			0.8			0.8		V
V_I	Input voltage	B port			V_{CC} (3.3 V)			V_{CC} (3.3 V)	V
		Except B port			5.5			5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+50 mV			V_{REF}+50 mV			V
		Except B port	2			2			
V_{IL}	Low-level input voltage	B port			V_{REF}–50 mV			V_{REF}–50 mV	V
		Except B port			0.8			0.8	
I_{IK}	Input clamp current				–18			–18	mA
I_{OH}	High-level output current	A port			–32			–32	mA
I_{OL}	Low-level output current	A port			64			64	mA
		B port			40			40	
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54GTL16616			SN74GTL16616			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	A port	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA	V_{CC}–0.2			V_{CC}–0.2			V
		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OH} = –8 mA	2.4			2.4			
			I_{OH} = –32 mA	2			2			
V_{OL}	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 64 mA			0.55			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V, I_{OL} = 40 mA				0.4			0.4	
I_I	Control inputs	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10			10	µA
	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			1			1	
			V_I = 0			–30			–30	
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = V_{CC} (3.3 V)			5			5	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0, V_I or V_O = 0 to 4.5 V				100			100	µA
$I_{I(hold)}$	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	–75			–75			
I_{OZH}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 3 V				1			1	µA
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 1.2 V				10			10	
I_{OZL}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 0.5 V				–1			–1	µA
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 0.4 V				–10			–10	
I_{CC} (3.3V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND	Outputs high			1			1	mA
			Outputs low			5			5	
			Outputs disabled			1			1	
I_{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND	Outputs high			120			120	mA
			Outputs low			120			120	
			Outputs disabled			120			120	
ΔI_{CC}§		V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, A or control inputs at V_{CC} (3.3 V) or GND, One input at 2.7 V				1			1	mA
C_i	Control inputs	V_I = 3.15 V or 0			3.5			3.5		pF
C_{io}	A port	V_O = 3.15 V or 0			12			12		pF
	B port	Per IEEE 1194.1				5			5	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

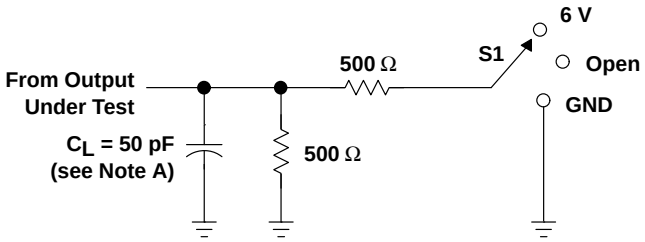
			SN54GTL16616		SN74GTL16616		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	95	0	95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		3.3		ns
		CLKAB or CLKBA high or low	5.5		5.5		
t_{su}	Setup time	A before CLKAB↑	1.1		1.1		ns
		B before CLKBA↑	2.6		2.6		
		A before LEAB↓	0		0		
		B before LEBA↓	1		1		
		$\overline{CEAB}$ before CLKAB↑	1.8		1.8		
		$\overline{CEBA}$ before CLKBA↑	2.1		2.1		
t_h	Hold time	A after CLKAB↑	1.6		1.6		ns
		B after CLKBA↑	0.2		0.2		
		A after LEAB↓	4.3		4.3		
		B after LEBA↓	2.8		2.8		
		$\overline{CEAB}$ after CLKAB↑	0.8		0.8		
		$\overline{CEBA}$ after CLKBA↑	0.7		0.7		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (see Figure 1)

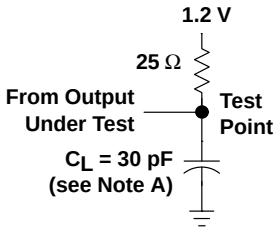
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16616			SN74GTL16616			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			95			95			MHz
t_{PLH}	A	B	1	2.5	3.8	1	2.5	3.8	ns
t_{PHL}			1	2	3.8	1	2	3.8	
t_{PLH}	LEAB	B	1.5	3.4	5.1	1.5	3.4	5.1	ns
t_{PHL}			1.4	3.2	5.1	1.4	3.2	5.1	
t_{PLH}	CLKAB	B	1.5	3.6	5	1.5	3.6	5	ns
t_{PHL}			1.4	4.1	5	1.4	4.1	5	
t_{PLH}	CLKAB	CLKOUT	3.4	6	7.7	3.4	6	7.7	ns
t_{PHL}			4.3	7.4	10.4	4.3	7.4	10.4	
t_{PLH}	$\overline{OEAB}$	B or CLKOUT	1.3	3.2	5	1.3	3.2	5	ns
t_{PHL}			1.1	3.1	5	1.1	3.1	5	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.2			1.2		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.7			0.7		ns
t_{PLH}	B	A	2.1	4.4	6.5	2.1	4.4	6.5	ns
t_{PHL}			1.3	3.3	4.8	1.3	3.3	4.8	
t_{PLH}	LEBA	A	1.7	3.9	6	1.7	3.9	6	ns
t_{PHL}			1.3	3.3	4.6	1.3	3.3	4.6	
t_{PLH}	CLKBA	A	1.7	4.1	6.3	1.7	4.1	6.3	ns
t_{PHL}			1.4	3.6	5.3	1.4	3.6	5.3	
t_{PLH}	CLKOUT	CLKIN	6.5	10.5	14.3	6.5	10.5	14.3	ns
t_{PHL}			5.1	8.8	11.8	5.1	8.8	11.8	
t_{en}	$\overline{OEBA}$	A or CLKIN	1.8	4.7	6.9	1.8	4.7	6.9	ns
t_{dis}			2	4.7	6.7	2	4.7	6.7	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

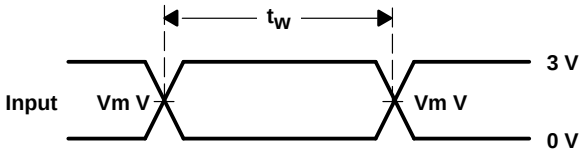


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

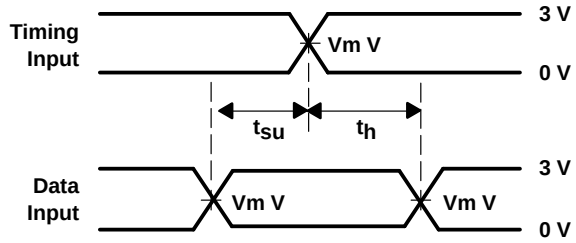


LOAD CIRCUIT FOR A OUTPUTS

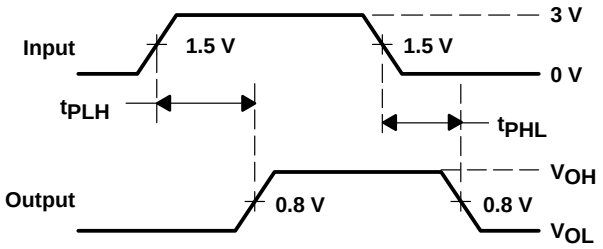
LOAD CIRCUIT FOR B OUTPUTS



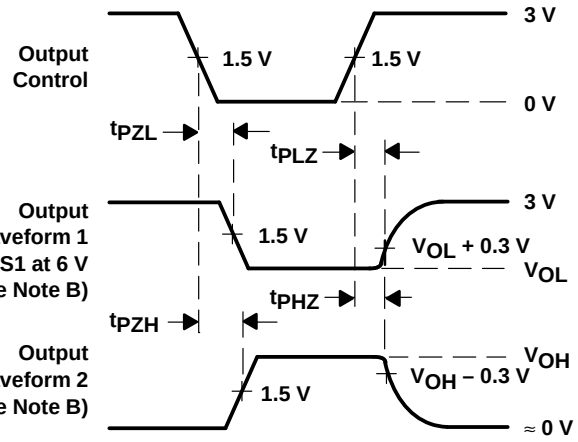
VOLTAGE WAVEFORMS
PULSE DURATION
(Vm = 1.5 V for A port and 0.8 V for B port)

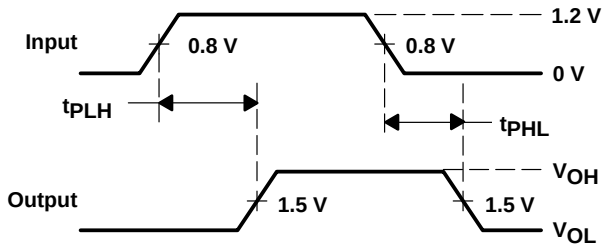


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(Vm = 1.5 V for A port and 0.8 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)





VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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