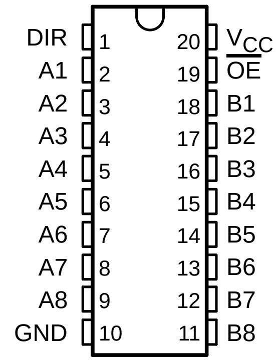
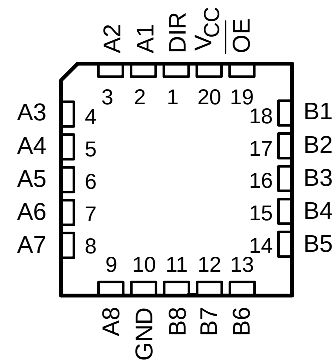
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **A-Bus Outputs Are Open Collector; B-Bus Outputs Are 3 State**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs (B Port) Eliminate the Need for External Pullup Resistors**
- **Support Live Insertion**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs**

SN54LVT639 . . . J PACKAGE
SN74LVT639 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT639 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These ′LVT639 are designed for asynchronous communication between open-collector and 3-state buses. These devices transmit data from the A bus (open collector) to the B bus (3 state) or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

Active bus-hold circuitry is provided on the B bus to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT639 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT639 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT639 is characterized for operation from –40°C to 85°C.

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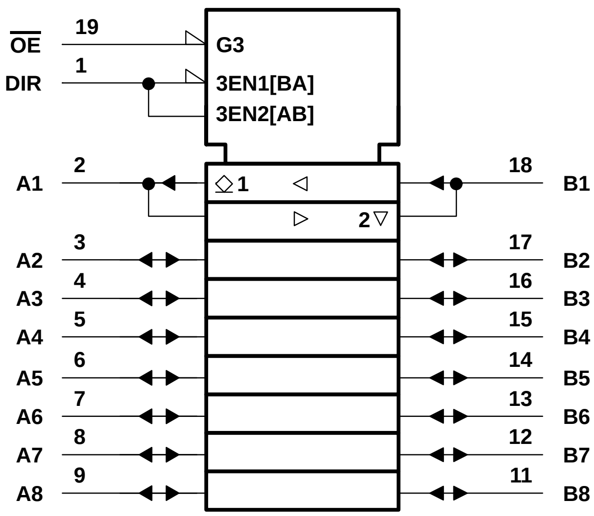
FUNCTION TABLE

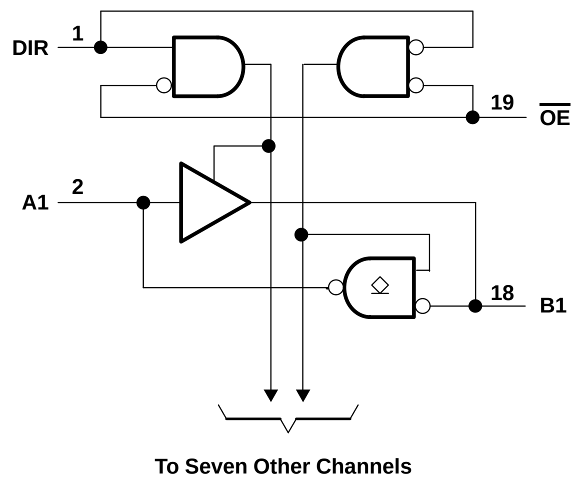
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT639	96 mA
SN74LVT639	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT639	48 mA
SN74LVT639	64 mA
Input clamp current, I_{IK} (V_I < 0)	–50 mA
Output clamp current, I_{OK} (V_O < 0)	–50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LVT639		SN74LVT639		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
V_{OH}	High-level output voltage	A port		3.6		3.6	V
I_{OH}	High-level output current	B port		–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT649 MIN	SN54LVT649 TYP†	SN54LVT649 MAX	SN74LVT649 MIN	SN74LVT649 TYP†	SN74LVT649 MAX	UNIT
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
I_{OH}	V_{CC} = 3 V,	V_{OH} = 3.6 V				20			20	µA
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control inputs			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			100			20	
		V_I = V_{CC}				5			5	
		V_I = 0				–10			–10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V	B port						±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	B port	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V	B port			1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V	B port			–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.5		0.13	0.19	mA
			Outputs low		8.8	14		8.8	12	
			Outputs disabled		0.13	0.5		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				10			10		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused terminals at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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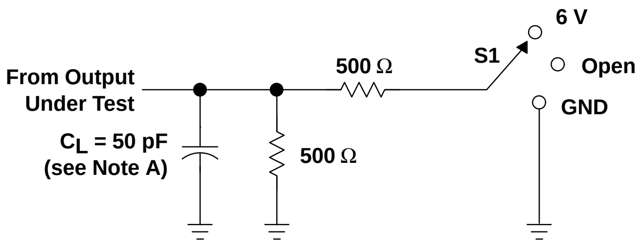
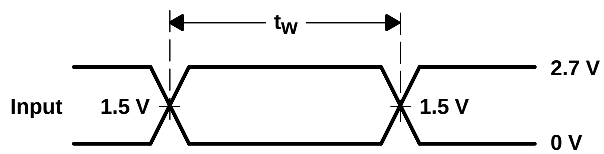
PARAMETER MEASUREMENT INFORMATION

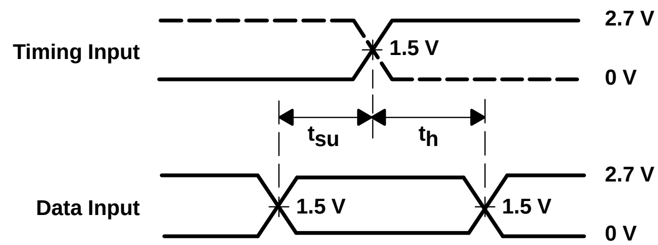


LOAD CIRCUIT FOR OUTPUTS

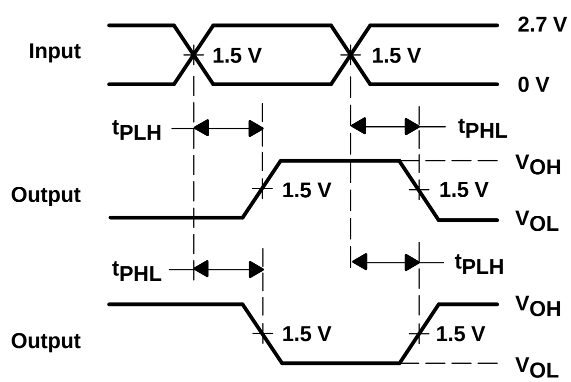
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



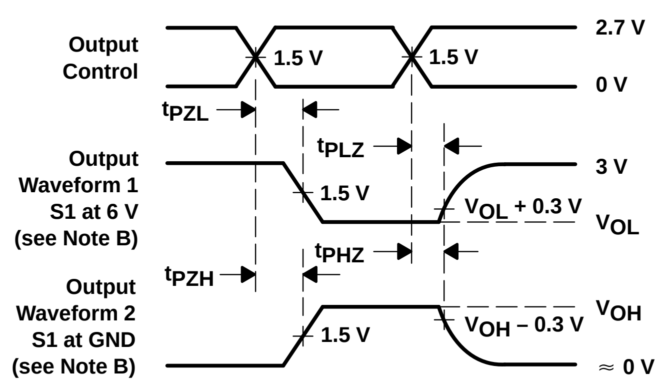
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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