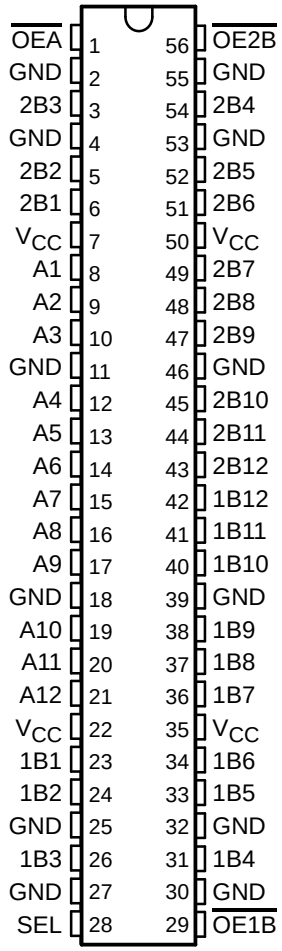
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$)**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings**

**SN54ABT16265 . . . WD PACKAGE**
**SN74ABT16265 . . . DL PACKAGE**
**(TOP VIEW)**




PRODUCT PREVIEW

## description

The ’ABT16265 is a 12-bit to 24-bit multiplexed transceiver used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. These control signals also allow byte-control of the most significant byte and least significant byte for each bus.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16265 is packaged in TI’s shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16265 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16265 is characterized for operation from –40°C to 85°C.

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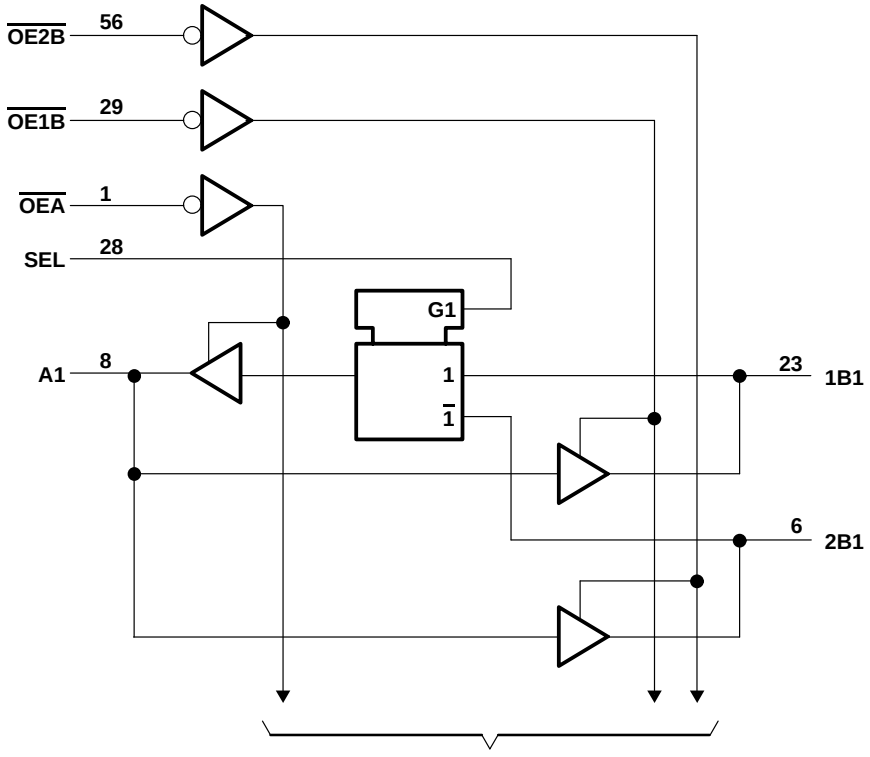
**FUNCTION TABLES**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| 1B | 2B | SEL | $\overline{OEA}$ | A |
| H | X | H | L | H |
| L | X | H | L | L |
| X | H | L | L | H |
| X | L | L | L | L |
| X | X | X | H | Z |

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| A | $\overline{OE1B}$ | $\overline{OE2B}$ | 1B | 2B |
| H | L | L | H | H |
| L | L | L | L | L |
| X | H | H | Z | Z |
| X | L | H | Active | Z |
| X | H | L | Z | Active |
| X | L | L | Active | Active |

PRODUCT PREVIEW

## logic diagram (positive logic)



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ . . . . . –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT16265 . . . . . 96 mA
SN74ABT16265 . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –18 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) . . . . . 1 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions

| | | | SN54ABT16265 | | SN74ABT16265 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

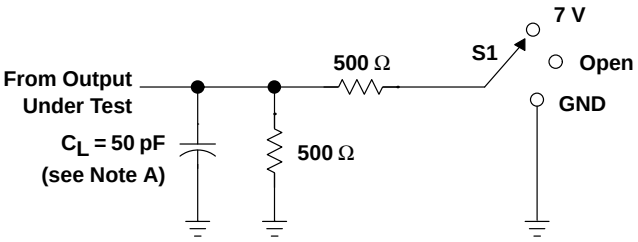
| PARAMETER | TEST CONDITIONS | | | $T_A$ = 25°C | | | SN54ABT16265 | | SN74ABT16265 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 3 mA | | 2.5 | | | 2.5 | | 2.5 | | V |
| | $V_{CC}$ = 5 V, | $I_{OH}$ = – 3 mA | | 3 | | | 3 | | 3 | | |
| | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 24 mA | | 2 | | | 2 | | | | |
| | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 32 mA | | 2‡ | | | | | 2 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 48 mA | | | | 0.55 | | 0.55 | | | V |
| | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 64 mA | | | | 0.55‡ | | | | 0.55 | |
| $I_I$ | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | Control inputs | | | ±1 | | ±1 | | ±1 | µA |
| | | | A or B ports | | | ±100 | | ±100 | | ±100 | |
| $I_{hold}$ | $V_{CC}$ = 4.5 V, | $V_I$ = 0.8 V | A or B ports | | | | | | 100 | | µA |
| | $V_{CC}$ = 4.5 V, | $V_I$ = 2 V | | | | | | | –100 | | |
| $I_{OZH}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 50 | | 50 | | 50 | µA |
| $I_{OZL}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | | –50 | | –50 | | –50 | µA |
| $I_{OFF}$ | $V_{CC}$ = 0 V, | $V_I$ or $V_O$ ≤ 4.5 V | | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | Outputs high | | | 50 | | 50 | | 50 | µA |
| $I_O$¶ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | | –50 | –100 | –180 | –50 | –180 | –50 | –180 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | Outputs high | | | 3 | | 3 | | 3 | mA |
| | | | Outputs low | | | 60 | | 60 | | 60 | |
| | | | Outputs disabled | | | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$# | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | Data inputs | Outputs enabled | | | 1 | | 1.5 | | 1 | mA |
| | | | Outputs disabled | | | 0.05 | | 0.05 | | 0.05 | |
| | | Control inputs | | | | 1.5 | | 1.5 | | 1.5 | |
| $C_i$ | $V_I$ = 2.5 V or 0.5 V | | Control inputs | | | | | | | | pF |
| $C_{io}$ | $V_O$ = 2.5 V or 0.5 V | | A or B ports | | | | | | | | pF |

† All typical values are at $V_{CC}$ = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

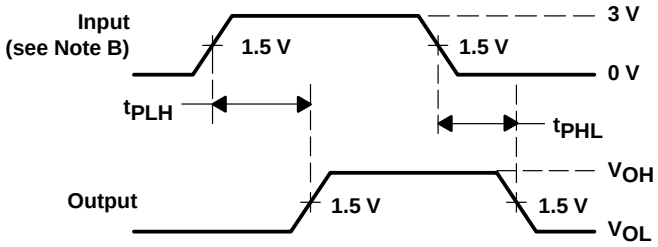
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT16265 | | SN74ABT16265 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | | | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | | |
| $t_{PLH}$ | SEL | A | | | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | | |
| $t_{PZH}$ | OE | A or B | | | | | | | | ns |
| $t_{PZL}$ | | | | | | | | | | |
| $t_{PHZ}$ | OE | A or B | | | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | | |

## PARAMETER MEASUREMENT INFORMATION

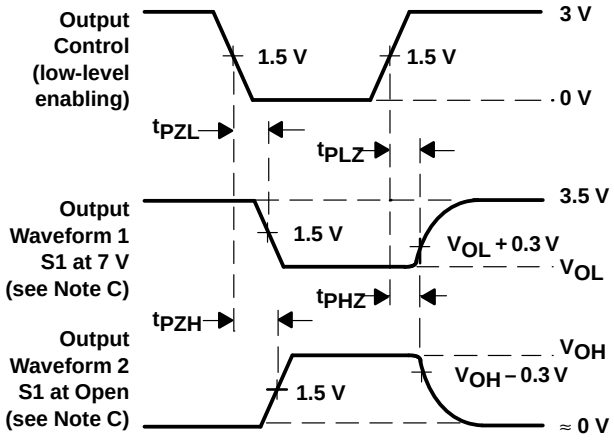



LOAD CIRCUIT FOR OUTPUTS

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

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