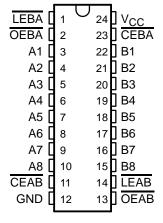
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- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C
- High-Drive Outputs (-32-mA I_{OH}, 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, and Standard Plastic 300-mil DIPs (JT)

DB, DW, OR NT PACKAGE (TOP VIEW)



description

The SN74ABT543A octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT543A is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74ABT543A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE†

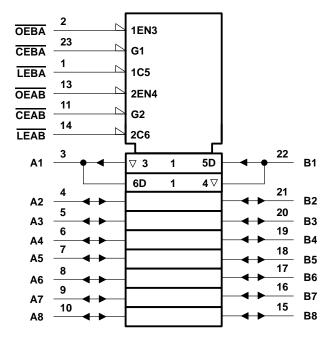
	OUTPUT			
CEAB	LEAB	OEAB	Α	В
Н	Х	Х	Х	Z
Х	Χ	Н	Χ	Z
L	Н	L	Χ	в ₀ ‡
L	L	L	L	L
L	L	L	Н	Н

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

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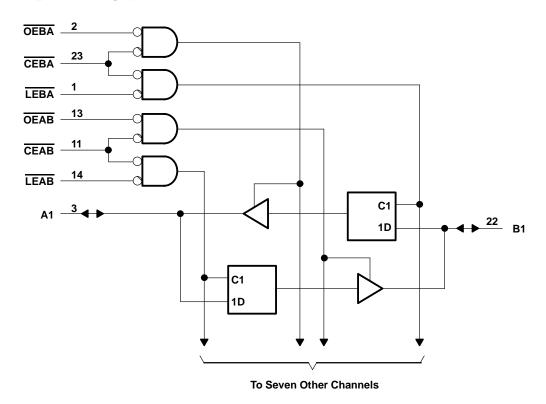
[‡] Output level before the indicated steady-state input conditions were established.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN74ABT543A OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		-0.5 V to $7 V$
Input voltage range, V _I (except I/O ports) (see Note 1)	\dots -0.5 V to 7 V
Voltage range applied to any output in the high state of	or power-off state, VO	−0.5 V to 5.5 V
Current into any output in the low state, I _O		128 mA
Input clamp current, I _{IK} (V _I < 0)		
Output clamp current, I _{OK} (V _O < 0)		50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air):	DB package	0.7 W
	DW package	1 W
	NT package	1.3 W
Storage temperature range		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V _{CC} Supply voltage			4.5	5.5	V
VIH	High-level input voltage		2		V
VIL	Low-level input voltage			0.8	V
٧ _I	/ _I Input voltage			VCC	V
loh	High-level output current			-32	mA
loL	OL Low-level output current			64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

SN74ABT543A OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		Т	A = 25°C	;	MIN	MAY	UNIT	
PARAMETER		TEST CONDITIONS			TYP†		MAX		MAX
VIK	$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$				-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -3 mA		2.5			2.5		
Vari	$V_{CC} = 5 V$,	$I_{OH} = -3 \text{ mA}$		3			3		V
VOH	V _{CC} = 4.5 V	I _{OH} = -24 mA		2					V
	VCC = 4.5 V	$I_{OH} = -32 \text{ mA}$					2		
Voi	V _{CC} = 4.5 V	I _{OL} = 48 mA				0.55			V
VOL	VCC = 4.5 V	I _{OL} = 64 mA						0.55	V
l _l	V _{CC} = 5.5 V,	$V_1 = V_{CC}$ or GND $+$	Control inputs			±1		±1	μΑ
Ч			A or B ports			±100		±100	μΑ
I _{OZH} ‡	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.7 \text{ V}$				50		50	μΑ
I _{OZL} ‡	$V_{CC} = 5.5 \text{ V},$	V _O = 0.5 V				-50		-50	μΑ
IOFF	$V_{CC} = 0$,	V_I or $V_O \le 4.5 \text{ V}$				±100		±100	μΑ
ICEX	$V_{CC} = 5.5 \text{ V},$	V _O = 5.5 V	Outputs high			50		50	μΑ
ΙΟ§	$V_{CC} = 5.5 \text{ V},$	V _O = 2.5 V		-50	-100	-180	-50	-180	mA
	V _{CC} = 5.5 V,	A or B ports	Outputs high		1	250		250	μΑ
ICC	$I_{O} = 0$,		Outputs low		24	34		34	mA
	$V_I = V_{CC}$ or GND		Outputs disabled		0.5	250		250	μΑ
ΔI _{CC} ¶	$V_{CC} = 5.5 \text{ V},$ Other inputs at V_{CC}	One input at 3.4 V,				1.5		1.5	mA
C _i	V _I = 2.5 V or 0.5 V		Control inputs		4				pF
C _{io}	V _O = 2.5 V or 0.5 \	/	A or B ports		7				pF

[†] All typical values are at $V_{CC} = 5 \text{ V}$.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} = 5 V, T _A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
t _W	t _w Pulse duration, LEAB or LEBA low					3.5		ns
	Setup time	Data before LEAB or LEBA Data before CEAB or CEBA	High	2.5		2.5		ns
1.			Low	3		3		
t _{su}			High	2.5		2.5		
		Low		2.5		2.5		
4.	Hold time	Data after LEAB or LEBA↑		1		1		ns
th	Hold tillle	Data after CEAB or CEBA↑		1	·	1		115



[‡]The parameters I_{OZH} and I_{OZL} include the input leakage current.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

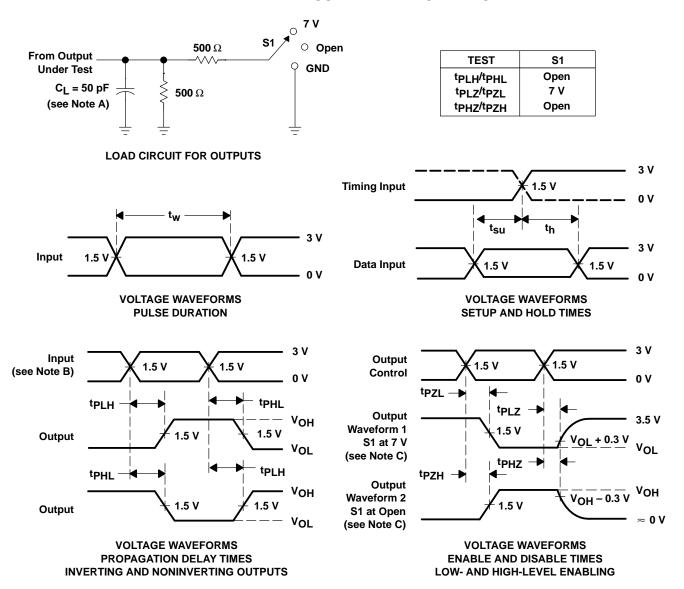
[¶] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			MIN	MAX	UNIT
	(INFOT)	(001701)	MIN	TYP	MAX			
^t PLH	A or B	B or A	1.6	3.3	4.4	1.6	5	ns
^t PHL	AOIB	BUIA	1.6	4.1	5.1	1.6	6	115
t _{PLH}	LEBA or LEAB	A or B	1.6	3.9	5.1	1.6	6.2	ns
t _{PHL}	LEBA or LEAB		1.6	4.4	5.4	1.6	6.3	110
^t PZH	OEBA or OEAB	A or B	1.4	3.1	4.1	1.4	5	ns
tPZL	OEBA OI OEAB	AOIB	2	3.9	4.9	2	5.7	110
^t PHZ	OEBA or OEAB	A or B	2.5	4.2	5.8	2.5	6.7	ns
t _{PLZ}	OEBA OI OEAB	AUID	2.5	4.8	6.1	2.5	7	115
^t PZH	CEBA or CEAB	A or B	1.4	3.4	4.4	1.4	5.4	ns
t _{PZL}	CEBA OF CEAB	AUID	2	4.1	5.2	2	6.1	115
^t PHZ	CEBA or CEAB	A or B	3.2	4.7	6.1	3.2	7	nc
tPLZ		AUID	2.5	5	6.7	2.5	7.3	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns. $t_f \leq 2.5$ ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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