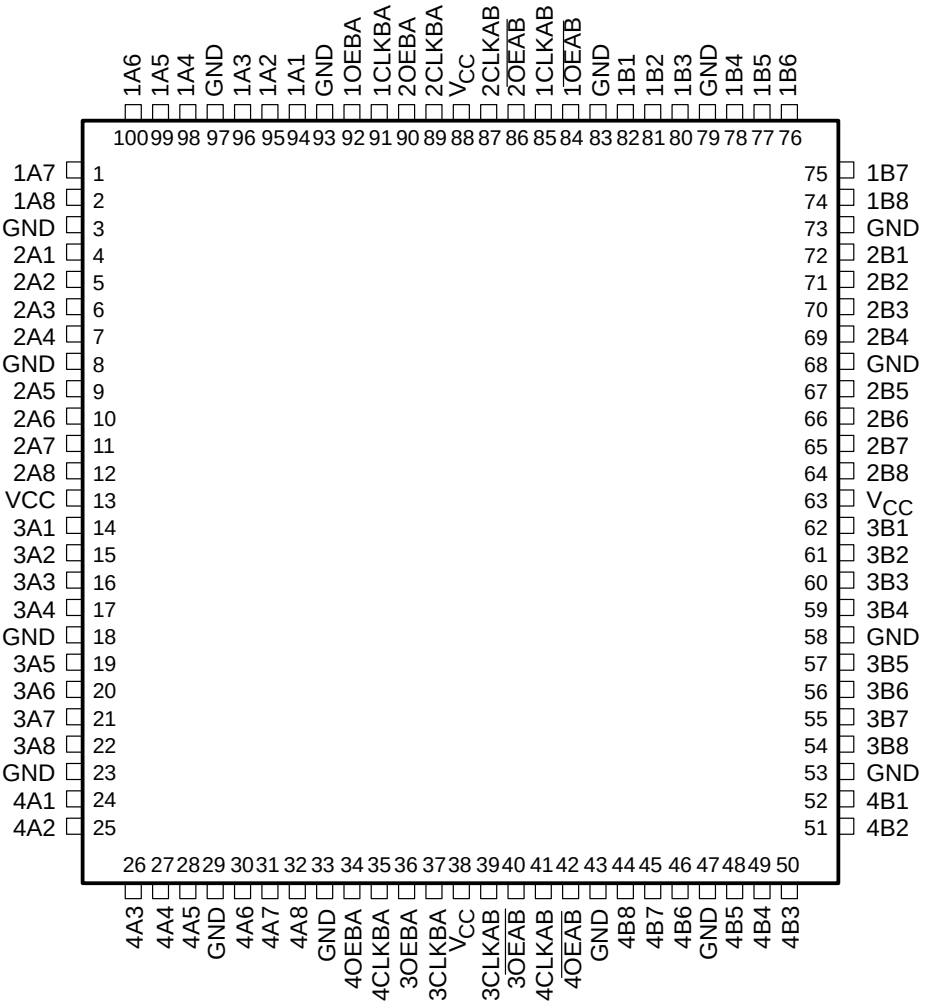
- **Members of the Texas Instruments *Widebus+*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Packaged in 100-Pin Plastic Shrink Quad Flat Pack (SQFP) With 14 × 14-mm Package Body Using 0.5-mm Lead Pitch**

SN74ABT32374 . . . PZ PACKAGE
(TOP VIEW)



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description

The ’ABT32374 is a 32-bit (quad 8-bit) transceiver with edge-triggered D-type flip-flops and 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ’ABT32374 can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. On the positive transition of the clock (CLKAB or CLKBA) input, the B outputs of the flip-flop take on the logic levels set up at the A inputs. The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the output-enable inputs.

A buffered output-enable ($\overline{\text{OEAB}}$ or OEBA) input can be used to place the 32 outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable ($\overline{\text{OEAB}}$ or OEBA) does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (A to B). OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (B to A).

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN54ABT32374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT32374 is characterized for operation from –40°C to 85°C.

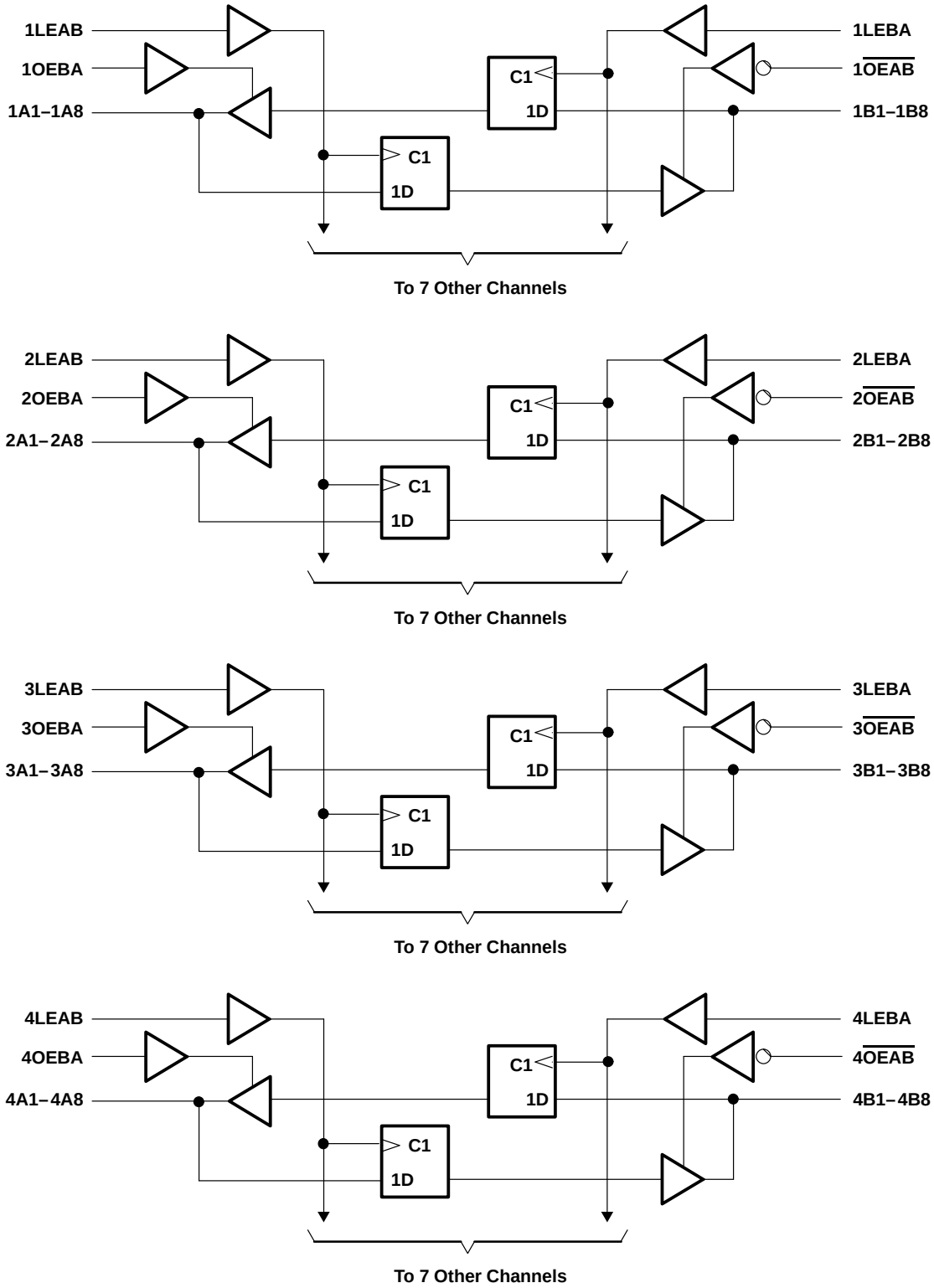
FUNCTION TABLE† (each flip-flop)

INPUTS			OUTPUT
$\overline{\text{OEAB}}$	CLKAB	A	B
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA and CLKBA.

PRODUCT PREVIEW

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT32374 . . . . . 96 mA
SN74ABT32374 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			SN54ABT32374		SN74ABT32374		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ABT32374			SN74ABT32374			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = –18 mA				–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = –3 mA		2.5			2.5			V
		V_{CC} = 5 V, I_{OH} = –3 mA		3			3			
		V_{CC} = 4.5 V, I_{OH} = –24 mA		2						
		V_{CC} = 4.5 V, I_{OH} = –32 mA					2			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55			0.55	V
		V_{CC} = 4.5 V, I_{OL} = 64 mA							0.55	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = V_{CC} or GND							±1	µA
	A or B ports								±100	
I_{hold}	A or B ports	V_{CC} = 4.5 V, V_I = 0.8 V					100			µA
		V_{CC} = 4.5 V, V_I = 2 V					–100			
I_{OZH}‡		V_{CC} = 5.5 V, V_O = 2.7 V							50	µA
I_{OZL}‡		V_{CC} = 5.5 V, V_O = 0.5 V							–50	µA
I_{OFF}		V_{CC} = 0, V_I or V_O ≤ 4.5 V							±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high						50	µA
I_O§		V_{CC} = 5.5 V, V_O = 2.5 V					–50	–100	–180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high						2	mA
			Outputs low						5	
			Outputs disabled						0.5	
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND							1	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V								pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V								pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54ABT32374		SN74ABT32374		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency					MHz
t_w	Pulse duration, CLK high or low					ns
t_{su}	Setup time, data before CLK↑					ns
t_h	Hold time, data after CLK↑					ns

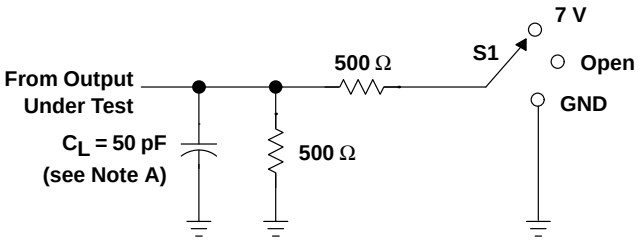
PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT32374			SN74ABT32374			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}									MHz
t_{PLH}	CLKAB or CLKBA	B or A							ns
t_{PHL}									
t_{PZH}	OEAB or OEBA	B or A							ns
t_{PZL}									
t_{PHZ}	OEAB or OEBA	B or A							ns
t_{PLZ}									

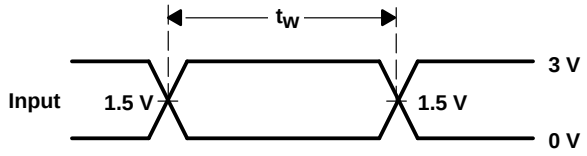
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

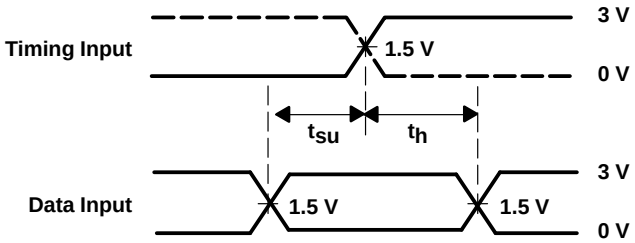


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

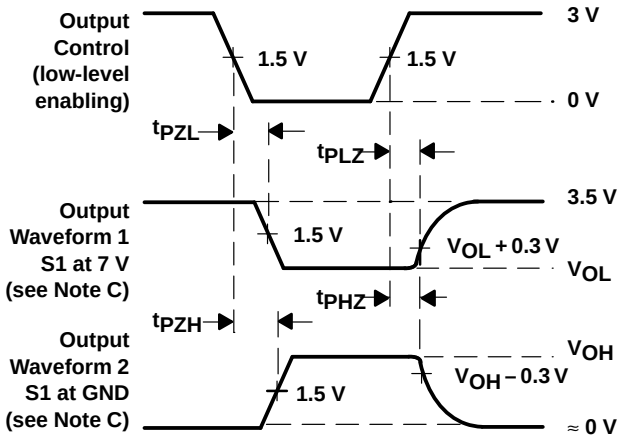
LOAD CIRCUIT FOR OUTPUTS



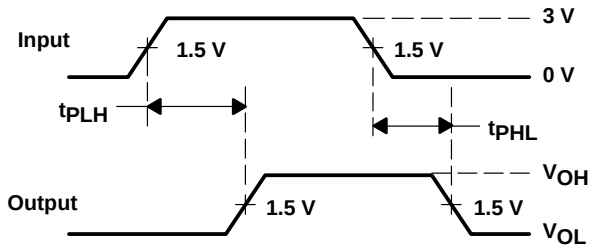
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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