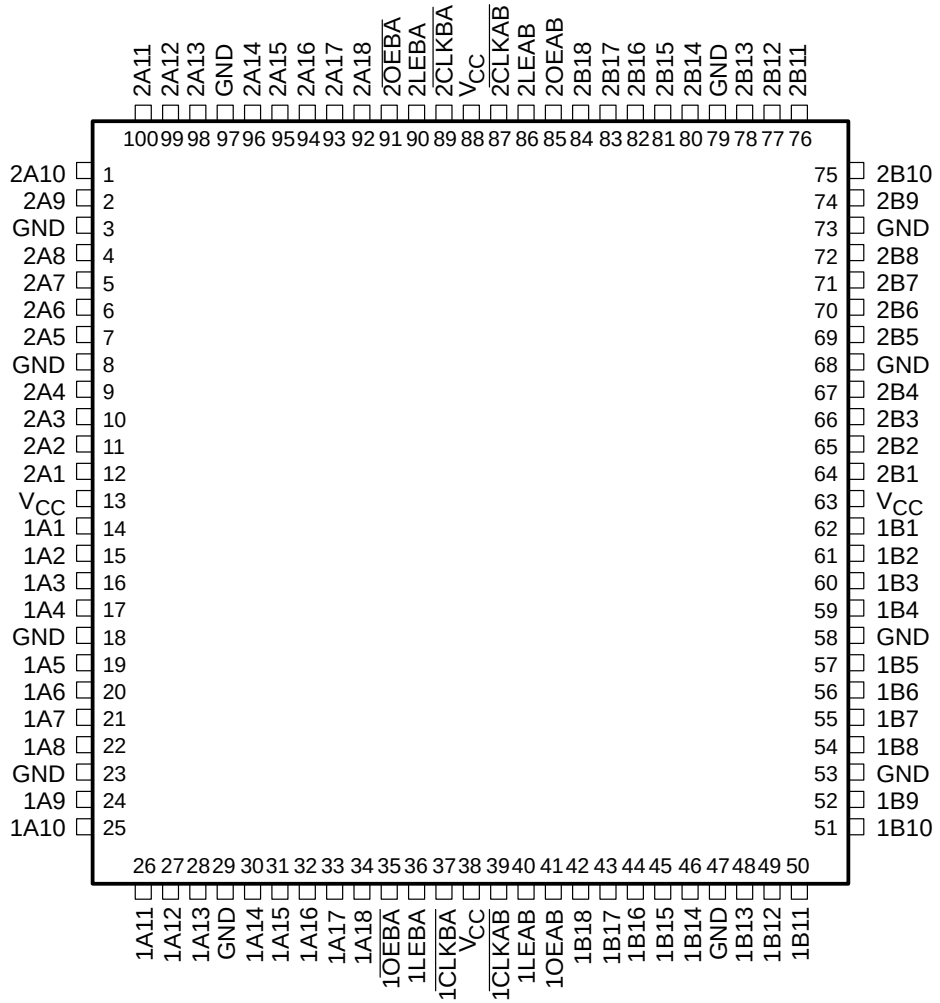
- **Members of the Texas Instruments *Widebus+*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in 100-Pin Plastic Shrink Quad Flat Pack (SQFP) With 14 × 14-mm Package Body Using 0.5-mm Lead Pitch**

SN74ABT32500 . . . PZ PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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description

These 36-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN54ABT32500 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT32500 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	$\overline{\text{CLKAB}}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

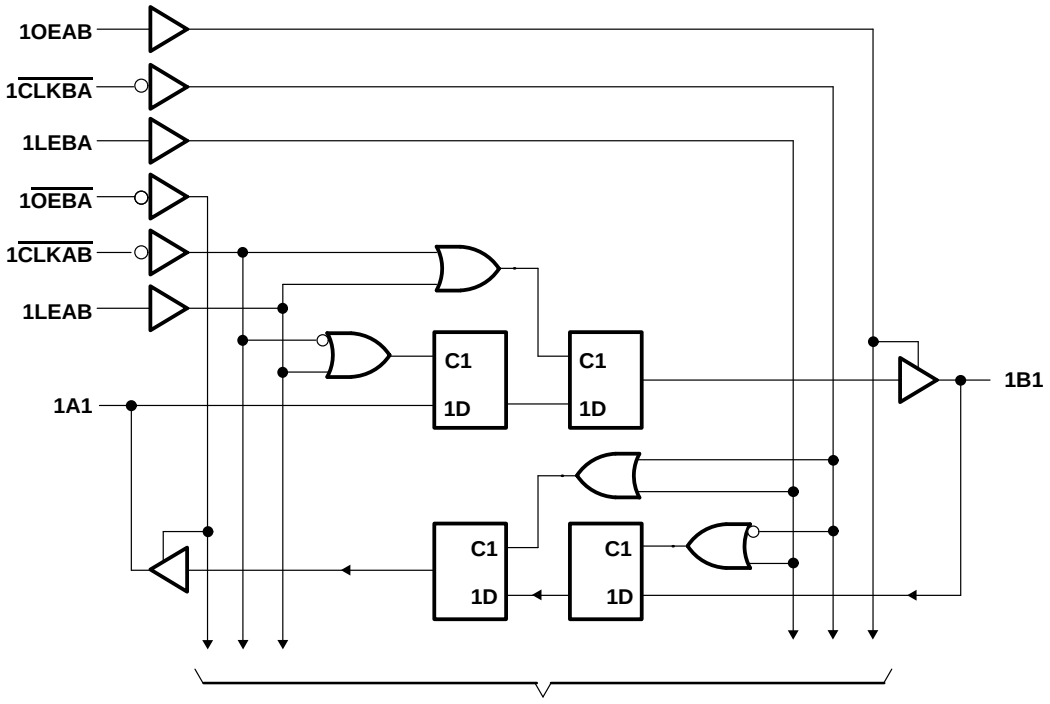
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.

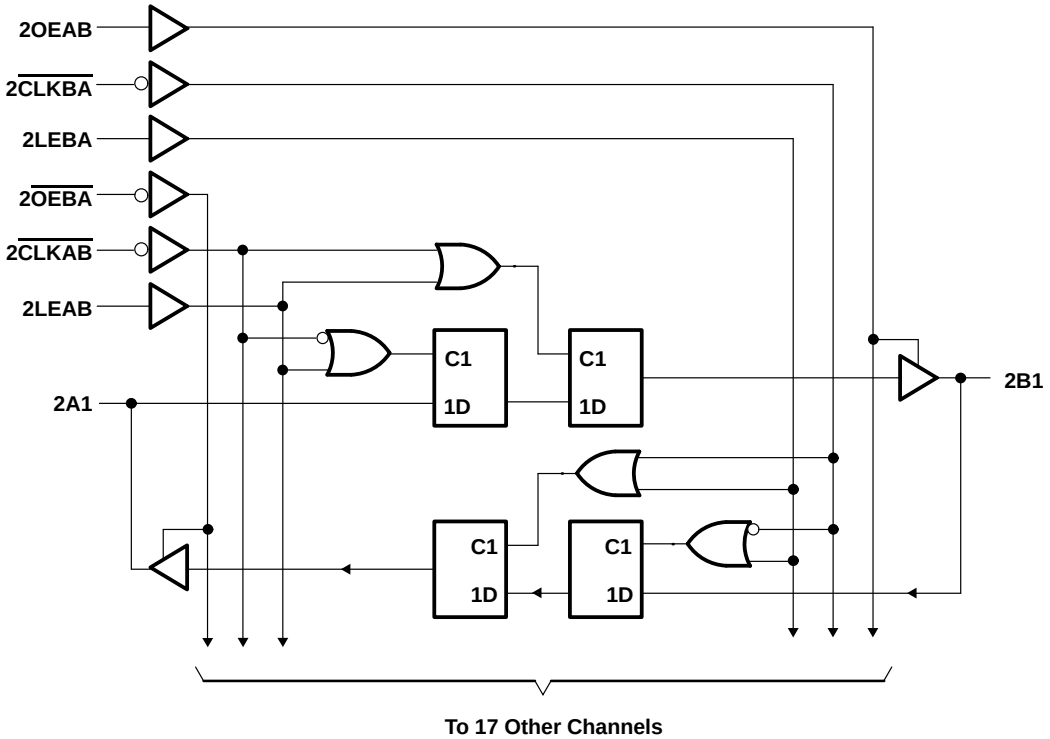
‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low.

PRODUCT PREVIEW

logic diagram (positive logic)





PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT32500 . . . . . 96 mA
SN74ABT32500 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT32500		SN74ABT32500		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ABT32500			SN74ABT32500			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = –18 mA				–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = –3 mA		2.5			2.5			V
		V_{CC} = 5 V, I_{OH} = –3 mA		3			3			
		V_{CC} = 4.5 V, I_{OH} = –24 mA		2						
		V_{CC} = 4.5 V, I_{OH} = –32 mA					2			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55			0.55	V
		V_{CC} = 4.5 V, I_{OL} = 64 mA							0.55	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = V_{CC} or GND							±1	µA
	A or B ports								±100	
I_{hold}	A or B ports	V_{CC} = 4.5 V, V_I = 0.8 V					100			µA
		V_{CC} = 4.5 V, V_I = 2 V								
I_{OZH}‡		V_{CC} = 5.5 V, V_O = 2.7 V							50	µA
I_{OZL}‡		V_{CC} = 5.5 V, V_O = 0.5 V							–50	µA
I_{OFF}		V_{CC} = 0, V_I or V_O ≤ 4.5 V							±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high						50	µA
I_O§		V_{CC} = 5.5 V, V_O = 2.5 V					–50	–100	–180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high						2	mA
			Outputs low						60	
			Outputs disabled						0.5	
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND							1	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V								pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V								pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT32500		SN74ABT32500		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency						MHz
t_w	Pulse duration	LE high					ns
		$\overline{CLK}$ high or low					
t_{su}	Setup time	A or B before $\overline{CLK}$↓					ns
		A or B before LE↓					
t_h	Hold time	A or B after $\overline{CLK}$↓					ns
		A or B after LE↓					

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT32500			SN74ABT32500			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}									MHz
t_{PLH}	A or B	B or A							ns
t_{PHL}									
t_{PLH}	LEAB or LEBA	B or A							ns
t_{PHL}									
t_{PLH}	CLKAB or CLKBA	B or A							ns
t_{PHL}									
t_{PZH}	OEAB or OEBA	B or A							ns
t_{PZL}									
t_{PHZ}	OEAB or OEBA	B or A							ns
t_{PLZ}									

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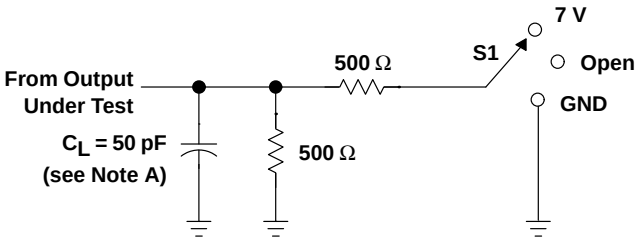
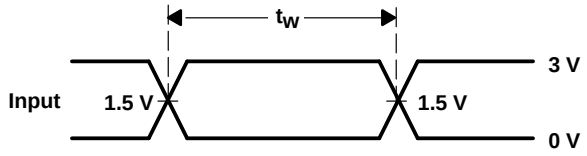
PARAMETER MEASUREMENT INFORMATION

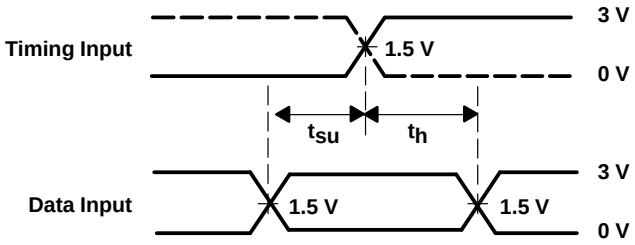


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

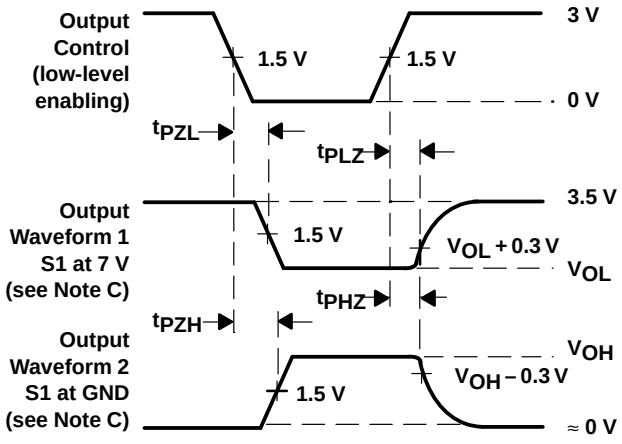
LOAD CIRCUIT FOR OUTPUTS



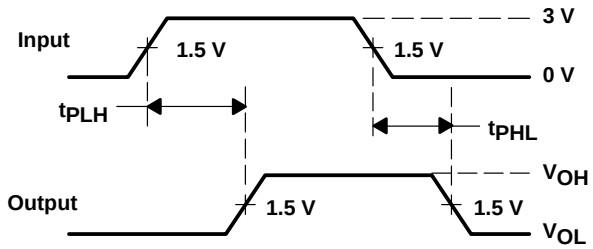
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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