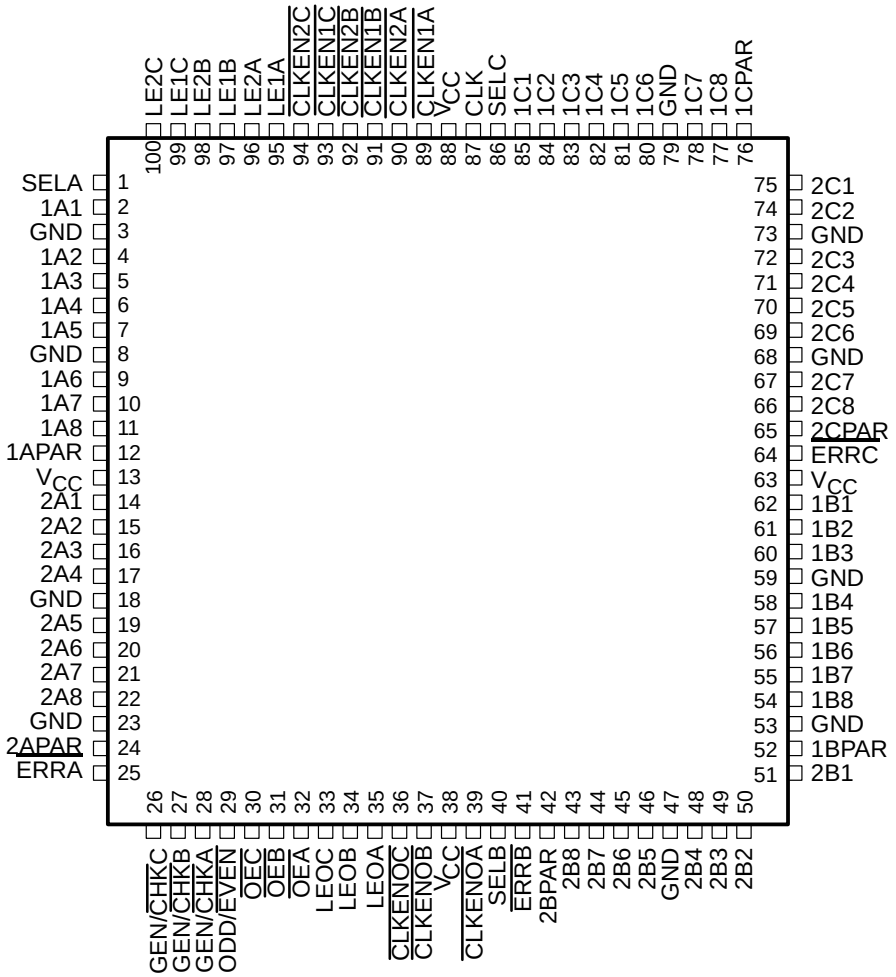
- **Member of the Texas Instruments *Widebus +*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBE*™ (Universal Bus Exchanger) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **Simultaneously Generates and Checks Parity**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Packaged in 100-Pin Plastic Thin Quad Flat Pack (TQFP) With 14 × 14-mm Package Body Using 0.5-mm Lead Pitch**

PCB PACKAGE
(TOP VIEW)



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description

The 'ABT32360 consists of three 16-bit registered input/output (I/O) ports. These registers combine D-type latches and flip-flops to allow data flow in transparent, latch, and clock modes. Data from one input port can be exchanged to one or more of the other ports. Because of the universal storage element, multiple combinations of real-time and stored data can be exchanged among the three ports.

Data flow in each direction is controlled by the output-enable ($\overline{OEA}$, $\overline{OEB}$, and $\overline{OEC}$), select-control (SELA, SELB, and SELC), latch-enable (LEA, LEB, and LEC), and clock enable ($\overline{CLKENA}$, $\overline{CLKENB}$, and $\overline{CLKENC}$) inputs. The A-data register operates in the transparent mode when LEA is high. When LEA is low, data is latched if CLK is held at a high or low logic level. If LEA and clock-enable A ($\overline{CLKENA}$) are low, data is stored on the low-to-high transition of CLKA. B and C ports operate identically. Output data selection is accomplished by the select-control pins. All three ports have active-low output enables, so when the output-enable input is low, the outputs are active (assuming LEO is high); when the output-enable input is high, the outputs are in the high-impedance state. Additionally, a synchronous output enable feature is provided which is activated when LEO is held low. If $\overline{CLKENO}$ is asserted, $\overline{OE}$ is activated on the rising edge of CLK and the outputs are enabled or disabled depending upon the level of $\overline{OE}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABT32360 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT32360 is characterized for operation from –40°C to 85°C.

OUTPUT FUNCTION TABLE†

INPUTS				OE INTERNAL STATUS	OUTPUT
$\overline{\text{CLKENO}}$	LEO	CLK	OE		
X	H	X	L	L	ACTIVE
X	H	X	H	H	Z
H	L	X	X	$\overline{OE}_0$‡	UNKNOWN¶
H	L	X	X	$\overline{OE}_0$‡	UNKNOWN¶
L	L	↑	L	L	ACTIVE
L	L	↑	H	H	Z
L	L	L	X	$\overline{OE}_0$‡	UNKNOWN¶
L	L	H	X	$\overline{OE}_0$§	UNKNOWN¶

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.
‡ Output level before the indicated steady-state input conditions were established.
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.
¶ Dependant upon $\overline{\text{OE}}$ prior to rising edge of CLK

STORAGE FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENA}}$	CLK	LEA	A	
H	X	L	X	Q_0‡
L	↑	L	L	L
L	↑	L	H	H
X	H	L	X	Q_0‡
X	L	L	X	Q_0‡
X	X	H	L	L
X	X	H	H	H

† A-port register shown. B and C ports are similar but use $\overline{\text{CLKENB}}$, $\overline{\text{CLKENC}}$, LEB, and LEC.
‡ Output level before the indicated steady-state input conditions were established.

PORT SELECT TABLES

INPUTS SELA	DATA PATH
L	B Register to Port A
H	C Register to Port A

INPUTS SELB	DATA PATH
L	C Register to Port B
H	A Register to Port B

INPUTS SELC	DATA PATH
L	A Register to Port C
H	B Register to Port C

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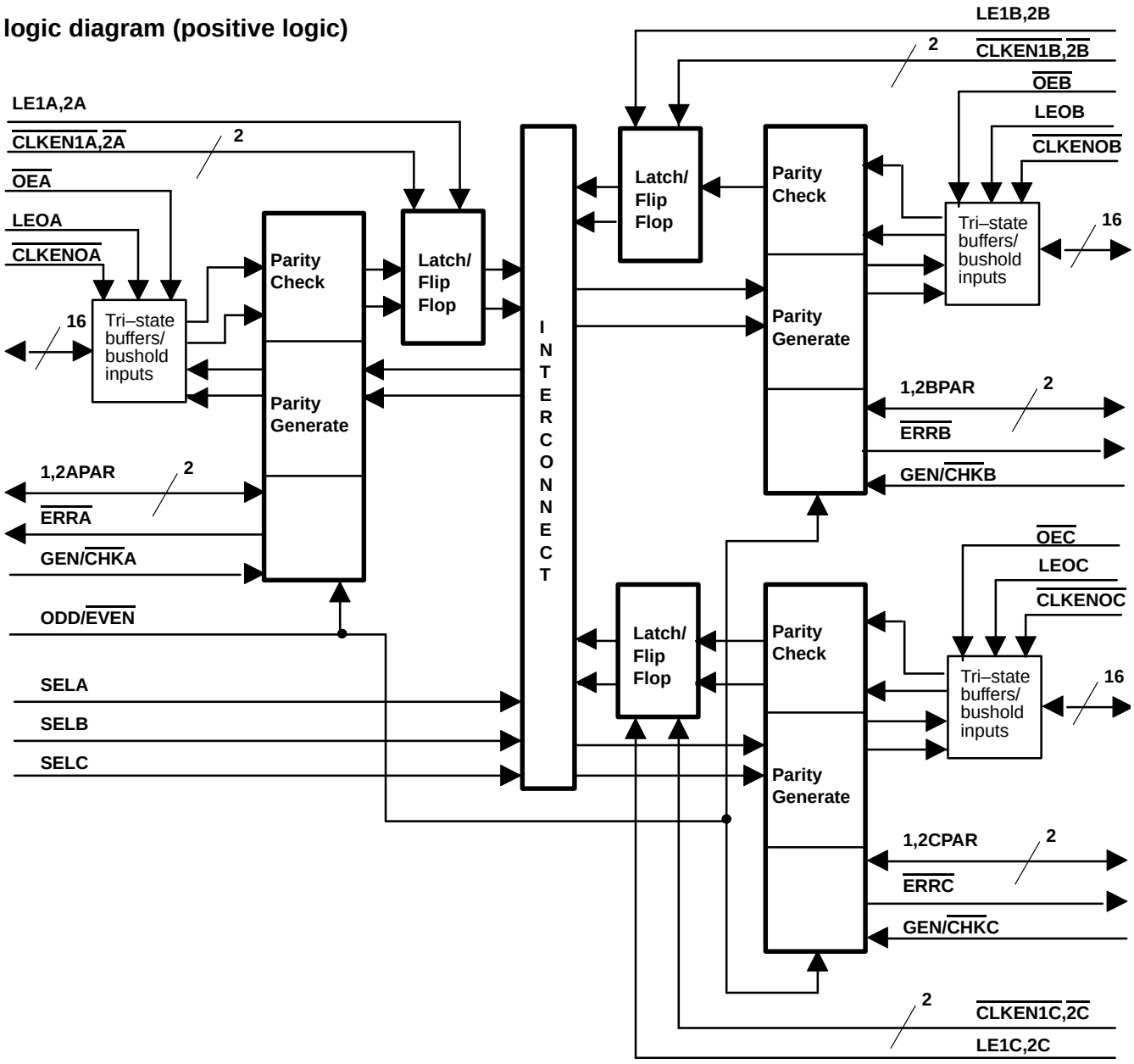
PARITY CONTROL FUNCTION TABLE

INPUTS			FUNCTION
$\overline{\text{GEN}}$/CHKA	$\overline{\text{GEN}}$/CHKB	$\overline{\text{GEN}}$/CHKC	
L	L	L	Parity of the data currently present on each of the ports is checked Errors are reported on $\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$, $\overline{\text{ERRC}}$
L	L	H	Parity of the data currently present on ports A and B are checked Errors are reported on $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ Parity is generated from the data currently present on port C
L	H	L	Parity of the data currently present on ports A and C are checked Errors are reported on $\overline{\text{ERRA}}$ and $\overline{\text{ERRC}}$ Parity is generated from the data currently present on port B
L	H	H	Parity of the data currently present on port A is checked Errors are reported on $\overline{\text{ERRA}}$ Parity bits 1,2BPAR and 1,2CPAR are generated from the current data on ports B and C
H	L	L	Parity of the data currently present on ports B and C are checked Errors are reported on $\overline{\text{ERRB}}$ and $\overline{\text{ERRC}}$ Parity bits 1,2APAR are generated from the data currently present on port A
H	L	H	Parity of the data currently present on port B is checked Errors are reported on $\overline{\text{ERRB}}$ Parity bits 1,2APAR and 1,2CPAR are generated from the current data on ports A and C
H	H	L	Parity of the data currently present on port C is checked Errors are reported on $\overline{\text{ERRC}}$ Parity bits 1,2APAR and 1,2BPAR are generated from the current data on ports A and C
H	H	H	Parity bits 1,2APAR, 1,2BPAR, and 1,2CPAR are generated from the current data on ports A, B, and C

PARITY FUNCTION TABLE

INPUTS				OUTPUTS	
ODD/$\overline{\text{EVEN}}$	Σ OF DATA BITS IN HIGH LOGIC STATE	$\overline{\text{GEN}}$/$\overline{\text{CHK}}$	PAR	PAR	$\overline{\text{ERR}}$
L	0, 2, 4, 6, 8	L	L	INPUT	H
L	1, 3, 5, 7	L	H	INPUT	H
L	0, 2, 4, 6, 8	L	H	INPUT	L
L	1, 3, 5, 7	L	L	INPUT	L
L	0, 2, 4, 6, 8	H	OUTPUT	L	X
L	1, 3, 5, 7	H	OUTPUT	H	X
H	0, 2, 4, 6, 8	L	L	INPUT	L
H	1, 3, 5, 7	L	H	INPUT	L
H	0, 2, 4, 6, 8	L	H	INPUT	H
H	1, 3, 5, 7	L	L	INPUT	H
H	0, 2, 4, 6, 8	H	OUTPUT	L	X
H	1, 3, 5, 7	H	OUTPUT	H	X

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at T_A = 55 °C (in still air): PZ package	1.2 W
Storage temperature range	–40°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{OH}	High-level output current			–32	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
T_A	Operating free-air temperature		–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			V
		V_{CC} = 5 V,	I_{OH} = –3 mA		3			
		V_{CC} = 4.5 V,	I_{OH} = –32 mA		2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA					V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1	µA
	A, B, or C ports						±100	
I_{hold}	A, B, or C ports	V_{CC} = 4.5 V,	V_I = 0.8 V		100			µA
		V_{CC} = 4.5 V,	V_I = 2 V		–100			
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V				50	µA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.5				–50	µA
I_{OFF}		V_{CC} = 0 V,	V_I or $V_O \le$ 5.5 V				±100	µA
I_{CEX}		V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50	µA
I_O§		V_{CC} = 5.5 V,	V_O = 2.5		–50	–100	–180	mA
I_{CC}		V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2	mA
				Outputs low			30	
				Outputs disabled			0.5	
ΔI_{CC}¶		V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V						pF
C_{io}	A, B, or C ports	V_O = 2.5 V or 0.5 V						pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

			MIN	MAX	UNIT
f_{clock}	Clock frequency				MHz
t_w	Pulse duration	LE high or low			ns
		CLK high or low			
t_{su}	Setup time	A, B, or C before CLK↑			ns
		$\overline{\text{CLKEN}}$ before CLK↑			
		A, B, or C before LE↓			ns

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t_h	Hold time	A, B, or C after CLK↑			ns
		$\overline{\text{CLKEN}}$ after CLK↑			
		A, B, or C after LE↓			ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}						MHz
t_{PLH}	A, B, or C	A, B, or C				ns
t_{PHL}						
t_{PLH}	A, B, or C	APAR, BPAR, or CPAR				ns
t_{PHL}						
t_{PLH}	APAR, BPAR, or CPAR	APAR, BPAR, or CPAR				ns
t_{PHL}						
t_{PLH}	A, APAR, B, BPAR, C, CPAR	ERRA, ERRB, or ERRC				ns
t_{PHL}						
t_{PLH}	ODD/EVEN	ERRA, ERRB, or ERRC				ns
t_{PHL}						
t_{PLH}	ODD/EVEN	APAR, BPAR, or CPAR				ns
t_{PHL}						
t_{PLH}	SEL	APAR, BPAR, or CPAR				ns
t_{PHL}						
t_{PLH}	CLK	A, B, or C				ns
t_{PHL}						
t_{PLH}	LEA, LEB, or LEC	A, B, or C				ns
t_{PHL}						
t_{PLH}	LEA, LEB, or LEC	APAR, BPAR, or CPAR (parity generated)				ns
t_{PHL}						
t_{PLH}	LEA, LEB, or LEC	ERRA, ERRB, or ERRC				ns
t_{PHL}						
t_{PLH}	LEOA, LEOB, or LEOC	A, B, or C				ns
t_{PHL}						
t_{PZH}	OE	A, B, or C				ns
t_{PZL}						
t_{PHZ}	OE	A, B, or C				ns
t_{PLZ}						
t_{PZH}	OE	PAR, ERR				ns
t_{PZL}						
t_{PHZ}	OE	PAR, ERR				ns
t_{PLZ}						

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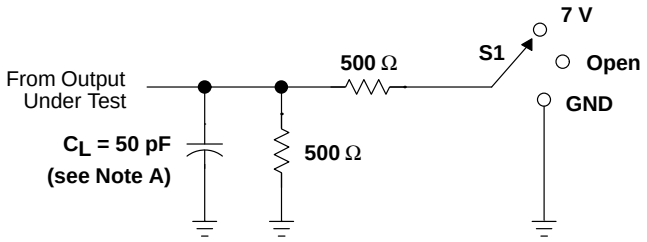
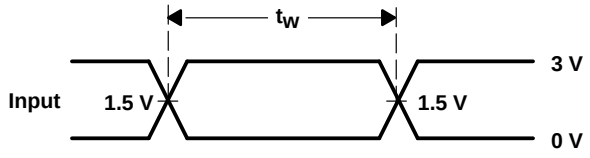
PARAMETER MEASUREMENT INFORMATION

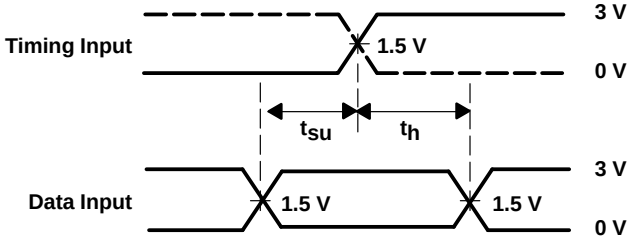


LOAD CIRCUIT FOR OUTPUTS

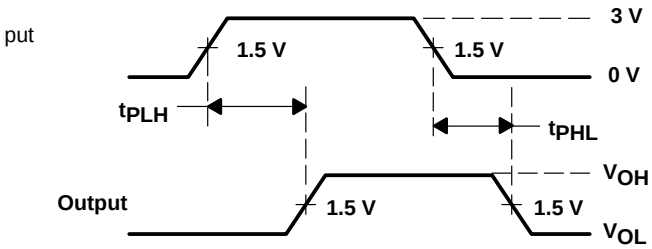
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 7 V GND



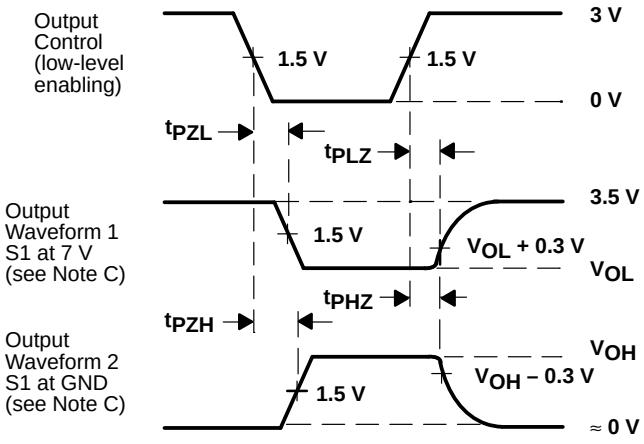
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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