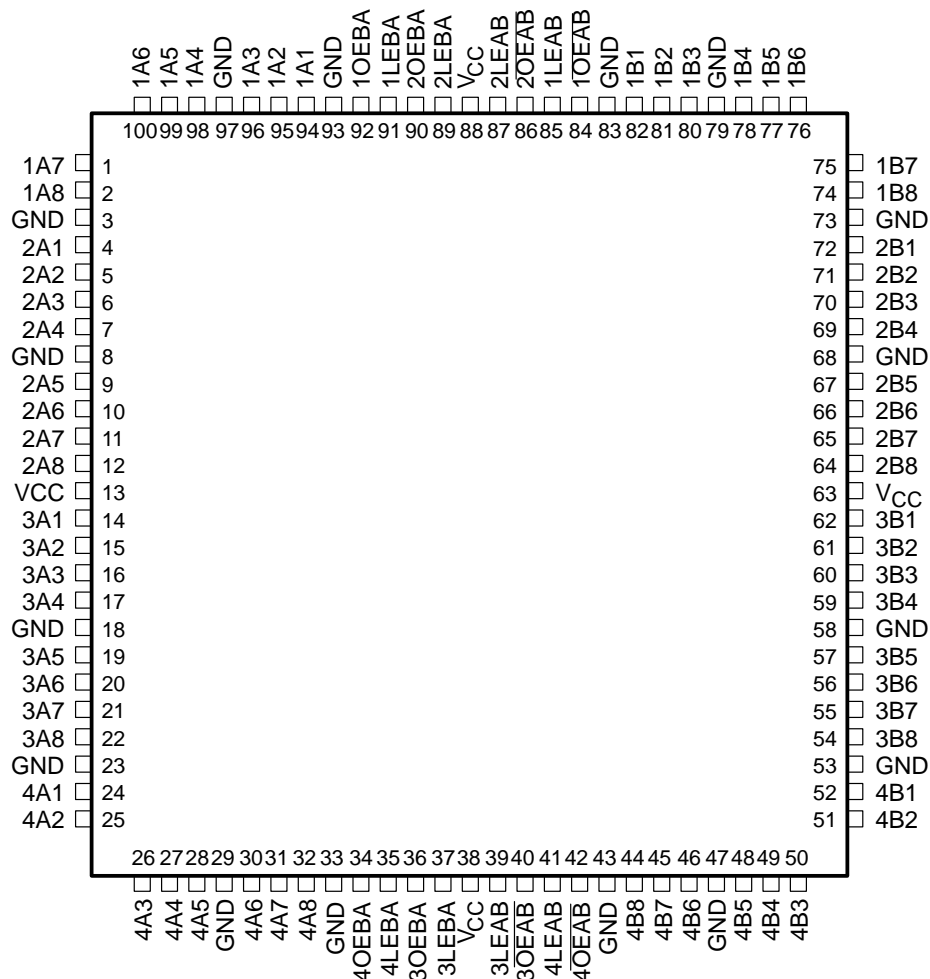


SN54ABT32373, SN74ABT32373 32-BIT TRANSCEIVERS WITH D-TYPE LATCHES AND 3-STATE OUTPUTS

SCBS460 – JUNE 1992–REVISED OCTOBER 1992

- Members of the Texas Instruments **Widebus+™** Family
- State-of-the-Art **EPIC-II^B™** BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Packaged in 100-Pin Plastic Shrink Quad Flat Pack (SQFP) With 14×14 -mm Package Body Using 0.5-mm Lead Pitch

SN74ABT32373 . . . PZ PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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SN54ABT32373, SN74ABT32373

32-BIT TRANSCEIVERS WITH D-TYPE LATCHES

AND 3-STATE OUTPUTS

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description

The 'ABT32373 is a 32-bit (quad 8-bit) transceiver with D-type latches and 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as four 8-bit transceivers, two 16-bit transceivers, or one 32-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the output-enable inputs.

The output-enable ($\overline{\text{OEAB}}$ or OEBA) inputs do not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (A to B). OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (B to A).

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN54ABT32373 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT32373 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†
(each transceiver)

INPUTS			OUTPUT
$\overline{\text{OEAB}}$	LEAB	A	B
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

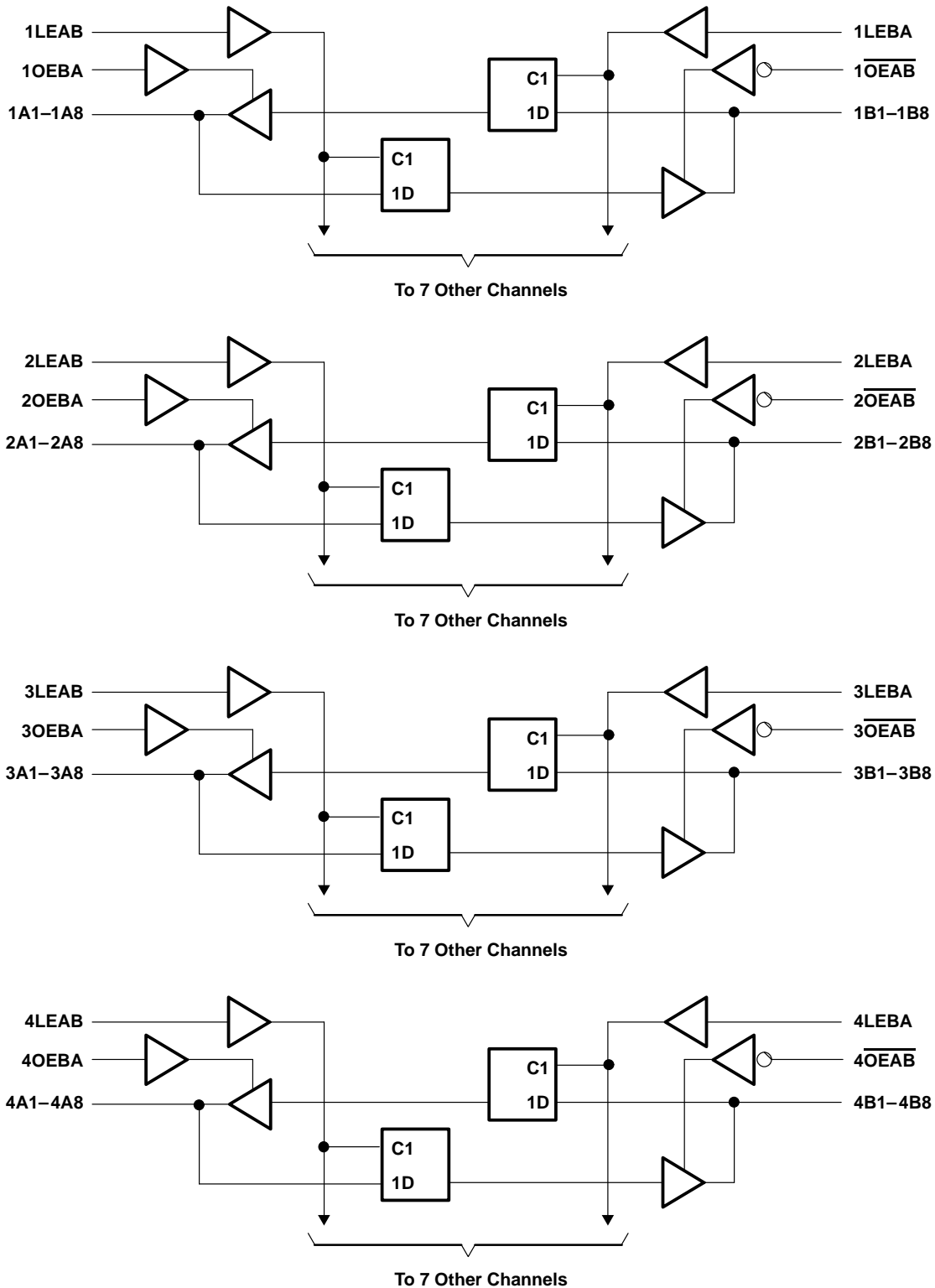
† A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA and LEBA.

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT32373	96 mA
SN74ABT32373	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		SN54ABT32373		SN74ABT32373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
	Outputs enabled					
T_A	Operating free-air temperature	–55	125	–40	85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ABT32373			SN74ABT32373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			2.5			V
		$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			3			
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -24\text{ mA}$	2						
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -32\text{ mA}$				2			
V_{OL}		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$			0.55			0.55	V
		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 64\text{ mA}$						0.55	
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$						± 1	μA
	A or B ports							± 100	
I_{hold}	A or B ports	$V_{CC} = 4.5\text{ V}$, $V_I = 0.8\text{ V}$				100			μA
		$V_{CC} = 4.5\text{ V}$, $V_I = 2\text{ V}$				-100			
I_{OZH}^\ddagger		$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$						50	μA
I_{OZL}^\ddagger		$V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$						-50	μA
I_{OFF}		$V_{CC} = 0$, $V_I\text{ or }V_O \leq 4.5\text{ V}$						± 100	μA
I_{CEX}		$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$						50	μA
I_{OS}^\S		$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$				-50	-100	-180	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$						2	mA
								5	
								0.5	
ΔI_{CC}^\P		$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$						1	mA
C_i	Control inputs	$V_I = 2.5\text{ V or }0.5\text{ V}$							pF
C_{io}	A or B ports	$V_O = 2.5\text{ V or }0.5\text{ V}$							pF

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54ABT32373		SN74ABT32373		UNIT
		MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high					ns
t_{su}	Setup time, data before LE↓					ns
t_h	Hold time, data after LE↓					ns

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SN54ABT32373, SN74ABT32373 **32-BIT TRANSCEIVERS WITH D-TYPE LATCHES** **AND 3-STATE OUTPUTS**

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

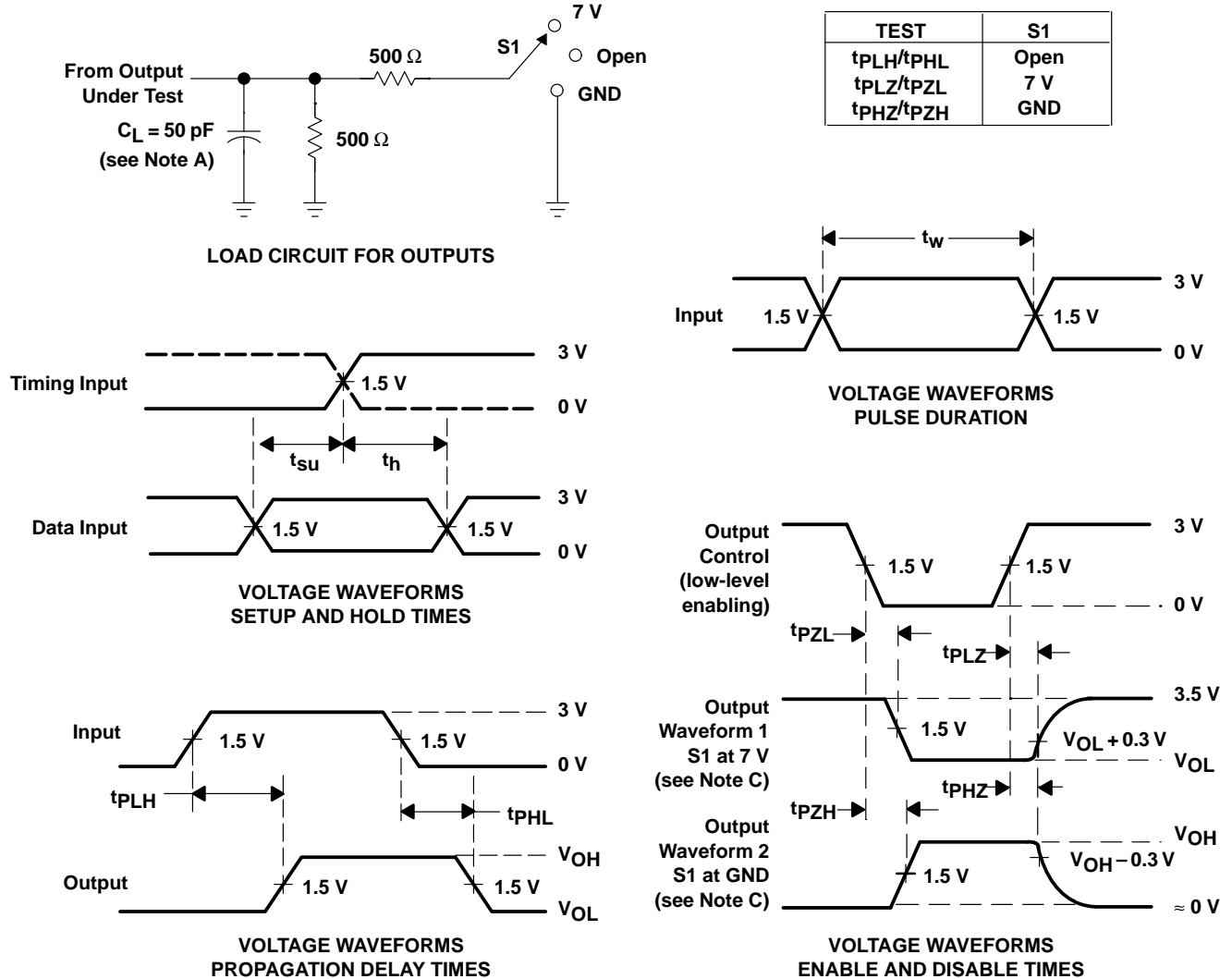
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT32373			SN74ABT32373			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A or B	B or A							ns
t_{PHL}									
t_{PLH}	LEAB or LEBA	B or A							ns
t_{PHL}									
t_{PZH}	OEAB or OEBA	B or A							ns
t_{PZL}									
t_{PHZ}	OEAB or OEBA	B or A							ns
t_{PLZ}									

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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