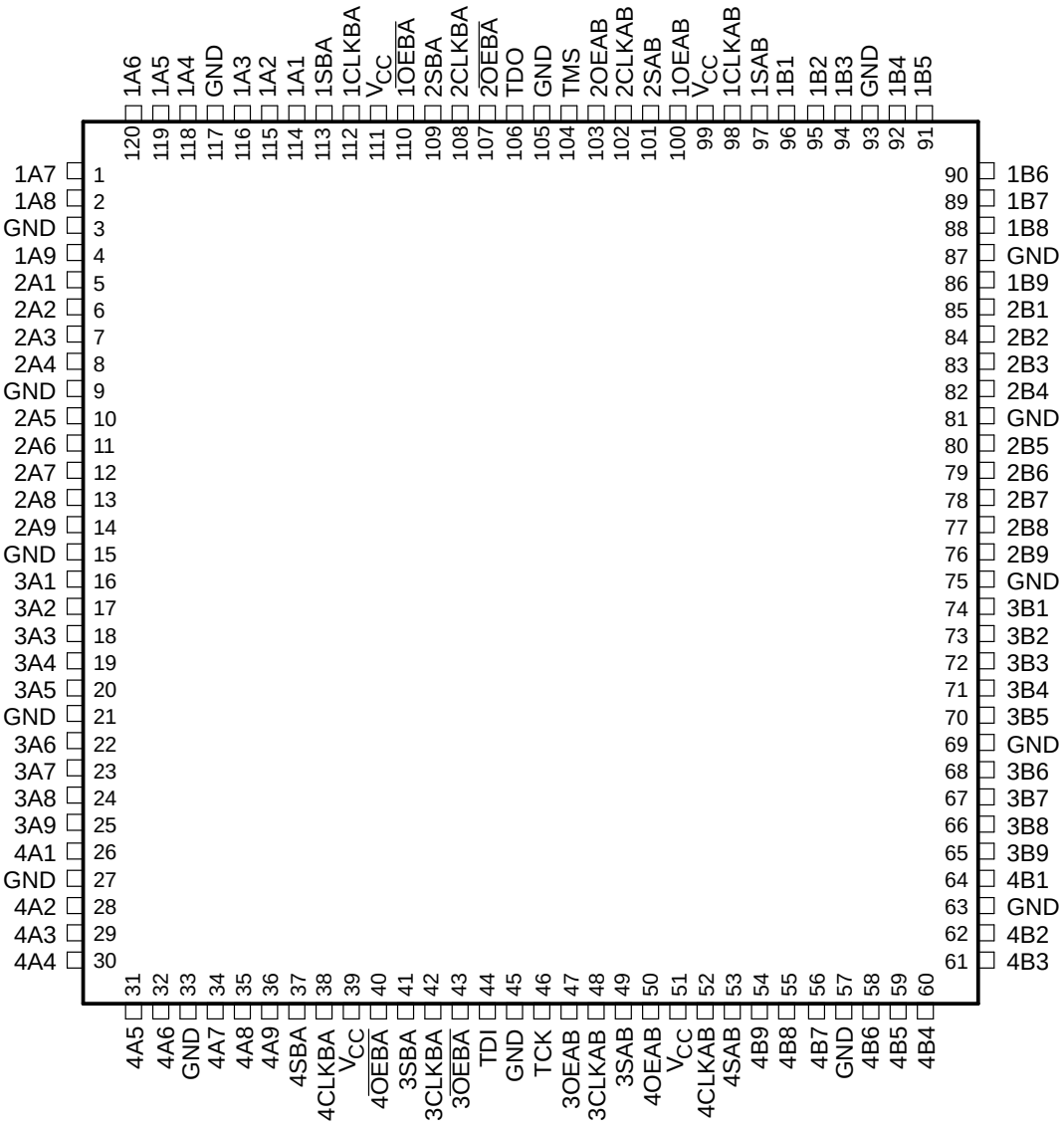
- **Member of the Texas Instruments *Widebus+*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Packaged in 120-Pin Cavity-Shrink Quad Flat Pack With 14 × 14-mm Package Body Using 0.4-mm Lead Pitch**

PACKAGE PINOUT
(TOP VIEW)



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description

The SN74ABT38652 is a 36-bit (quad 9-bit) bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. This device can be used as four 9-bit transceivers, two 18-bit transceivers, or one 36-bit transceiver.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ABT38652 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{\text{OEBA}}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.

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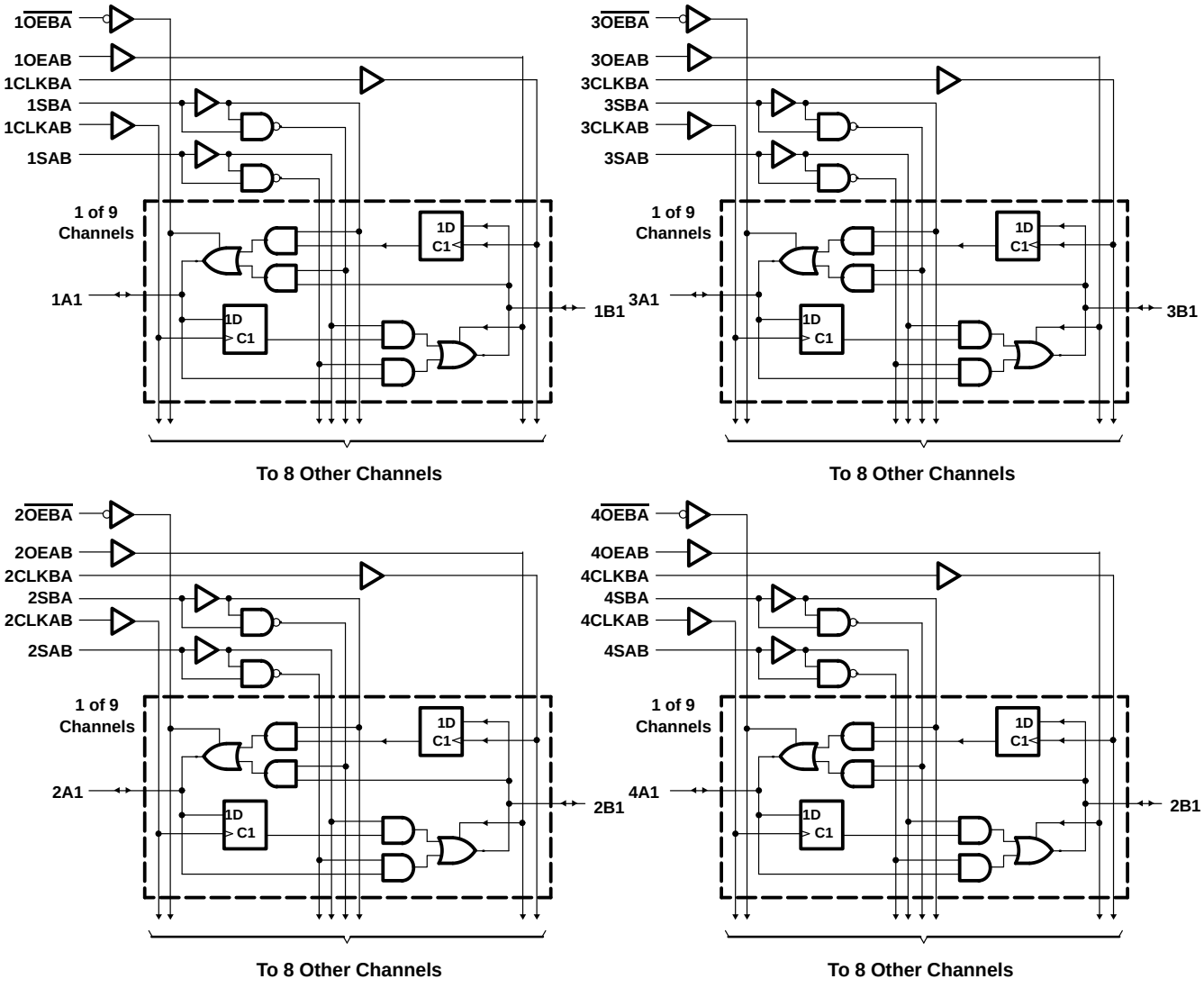
logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{OH}	High-level output current			–32	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
T_A	Operating free-air temperature		–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			V
		V_{CC} = 5 V,	I_{OH} = –3 mA		3			
		V_{CC} = 4.5 V,	I_{OH} = –32 mA		2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA					V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1	µA
	A or B ports						±100	
I_{hold}	A or B ports	V_{CC} = 4.5 V,	V_I = 0.8 V		100			µA
		V_{CC} = 4.5 V,	V_I = 2 V		–100			
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V				50	µA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.5 V				–50	µA
I_{OFF}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100	µA
I_{CEX}		V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50	µA
I_O§		V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	mA
I_{CC}		V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			4	mA
				Outputs low			60	
				Outputs disabled			0.5	
ΔI_{CC}¶		V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				0.5	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V						pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
f_{clock}	Clock frequency			MHz
t_w	Pulse duration, CLK high or low			ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑			ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑			ns

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}						MHz
t_{PLH}	CLKBA or CLKAB	A or B				ns
t_{PHL}						
t_{PLH}	A or B	B or A				ns
t_{PHL}						
t_{PLH}	SAB or SBA†	B or A				ns
t_{PHL}						
t_{PZH}	OEBA	A or B				ns
t_{PZL}						
t_{PHZ}	OEBA	A or B				ns
t_{PLZ}						
t_{PZH}	OEAB	A or B				ns
t_{PZL}						
t_{PHZ}	OEAB	A or B				ns
t_{PLZ}						

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

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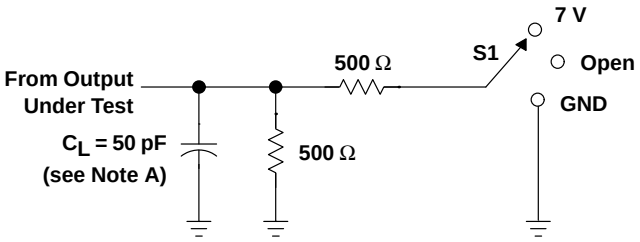
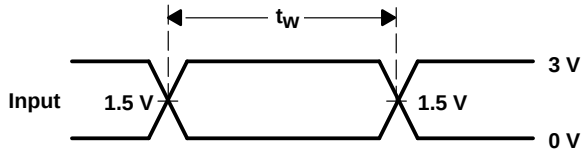
PARAMETER MEASUREMENT INFORMATION

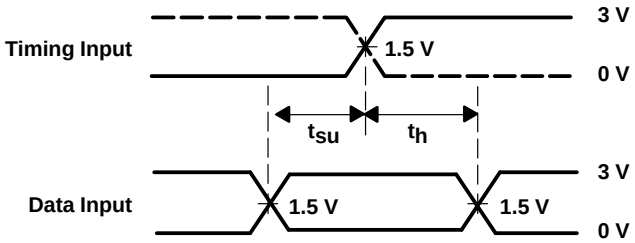


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

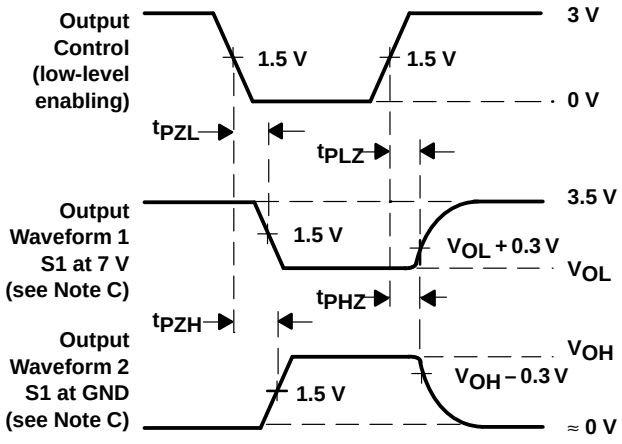
LOAD CIRCUIT FOR OUTPUTS



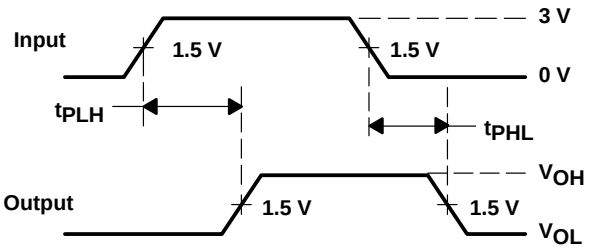
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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