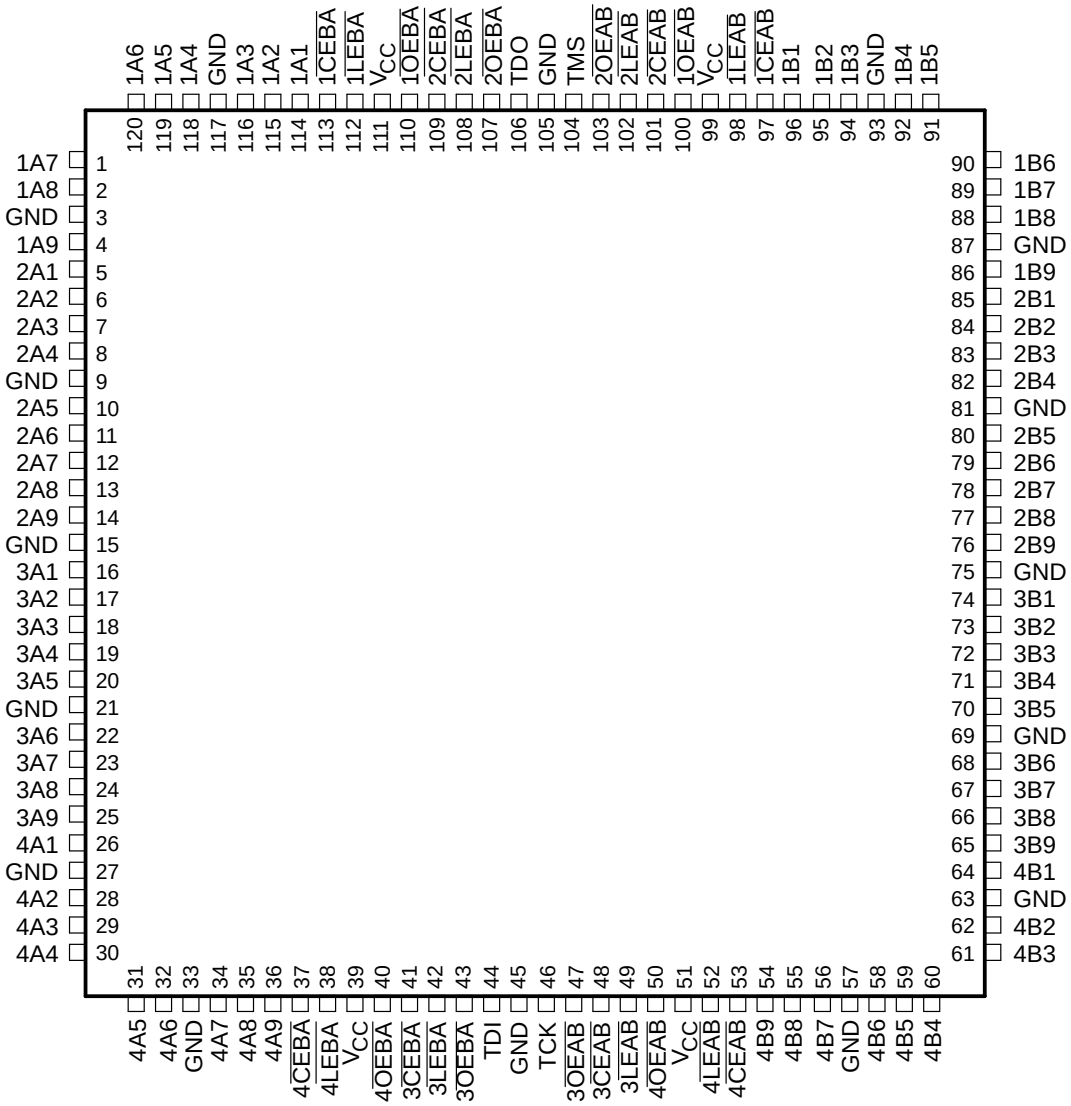
- **Member of the Texas Instruments *Widebus+*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Packaged in 120-Pin Cavity-Shrink Quad Flat Pack With 14 × 14-mm Package Body Using 0.4-mm Lead Pitch**

PACKAGE PINOUT
(TOP VIEW)



PRODUCT PREVIEW

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TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS
77251–1443

description

The SN74ABT38543 is a 36-bit (quad 9-bit) registered transceiver that contains four sets of D-type latches for temporary storage of data flowing in either direction. The device can be used as four 9-bit transceivers, two 18-bit transceivers, or one 36-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ABT38543 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE† (each 9-bit section)

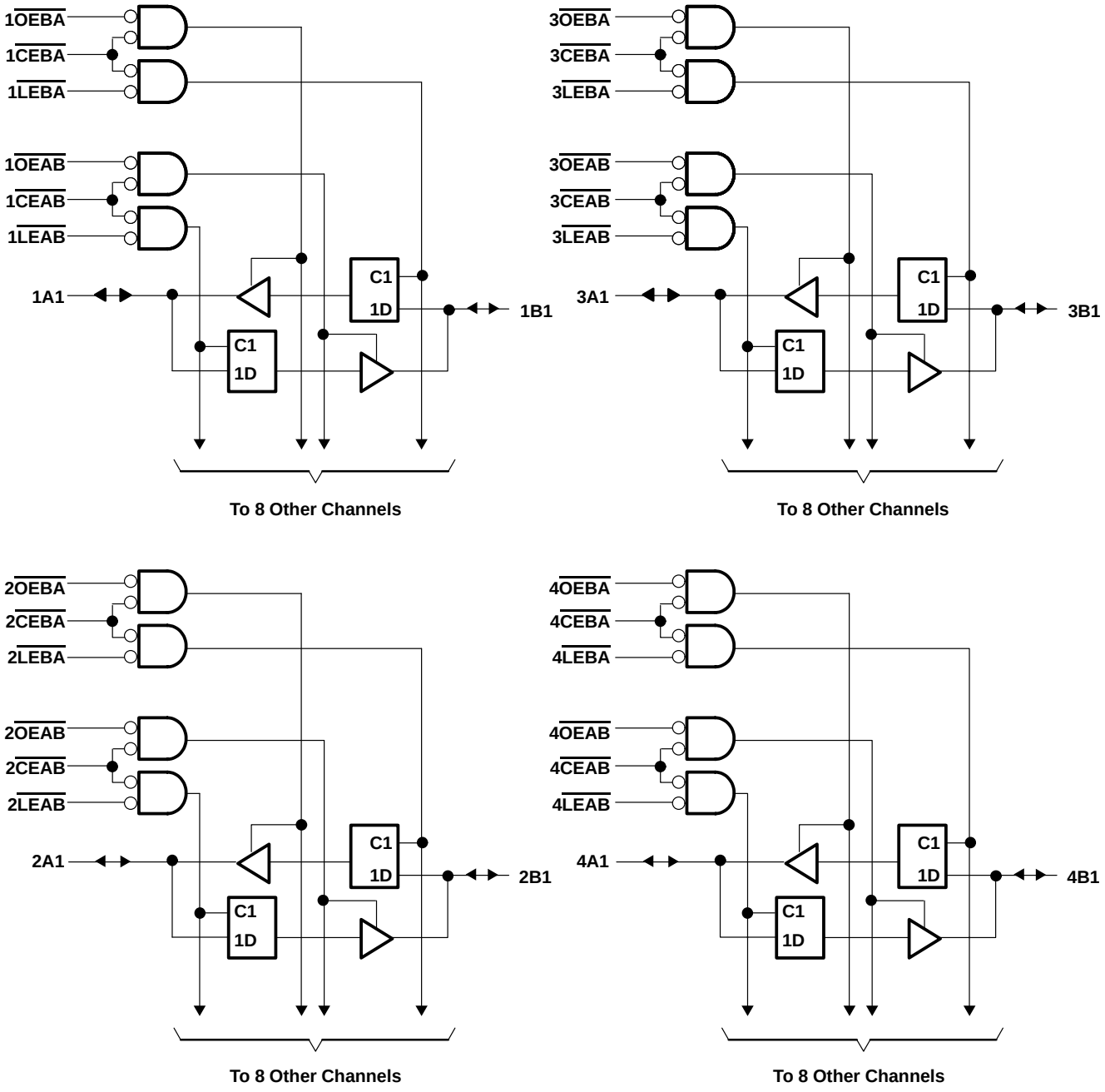
INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

‡ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{OH}	High-level output current			–32	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
T_A	Operating free-air temperature		–40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			V
		V_{CC} = 5 V,	I_{OH} = –3 mA		3			
		V_{CC} = 4.5 V,	I_{OH} = –32 mA		2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA					V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1	µA
	A or B ports						±100	
I_{hold}	A or B ports	V_{CC} = 4.5 V,	V_I = 0.8 V		100			µA
		V_{CC} = 4.5 V,	V_I = 2 V		–100			
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V				50	µA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.5 V				–50	µA
I_{OFF}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100	µA
I_{CEX}		V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50	µA
I_O§		V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	mA
I_{CC}		V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			4	mA
				Outputs low			60	
				Outputs disabled			0.5	
ΔI_{CC}¶		V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				0.5	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V						pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low				ns
t_{su}	Setup time	Data before $\overline{LEAB}$↑ or $\overline{LEBA}$↑			ns
		Data before $\overline{CEAB}$↑ or $\overline{CEBA}$↑			
t_h	Hold time	Data after $\overline{LEAB}$↑ or $\overline{LEBA}$↑			ns
		Data after $\overline{CEAB}$↑ or $\overline{CEBA}$↑			

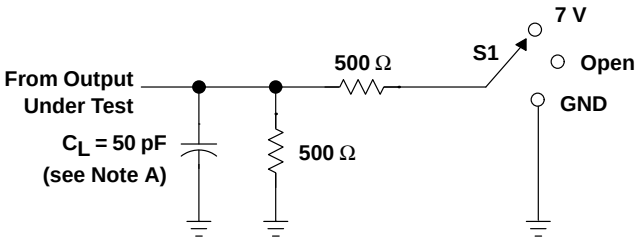
PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	B or A				ns
t_{PHL}						
t_{PLH}	LEBA or LEAB	A or B				ns
t_{PHL}						
t_{PHZ}	CEBA or CEAB	A or B				ns
t_{PLZ}						
t_{PZH}	CEBA or CEAB	A or B				ns
t_{PZL}						
t_{PHZ}	OEBA or OEAB	A or B				ns
t_{PLZ}						
t_{PZH}	OEBA or OEAB	A or B				ns
t_{PZL}						

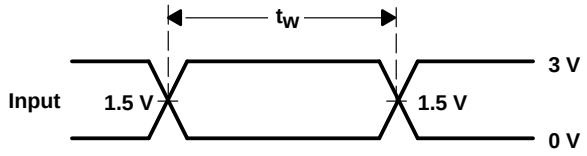
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

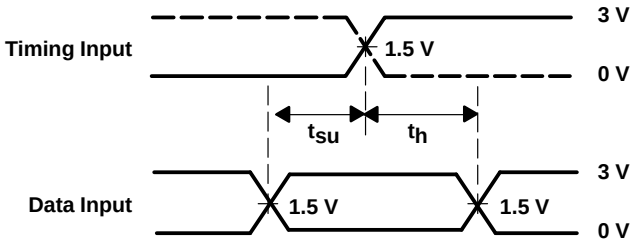


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

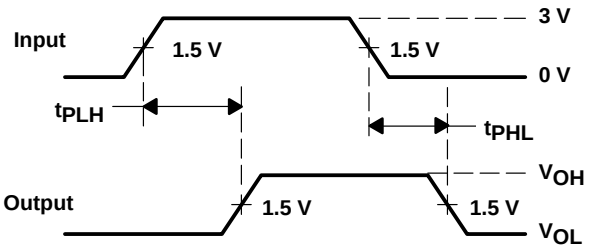
LOAD CIRCUIT FOR OUTPUTS



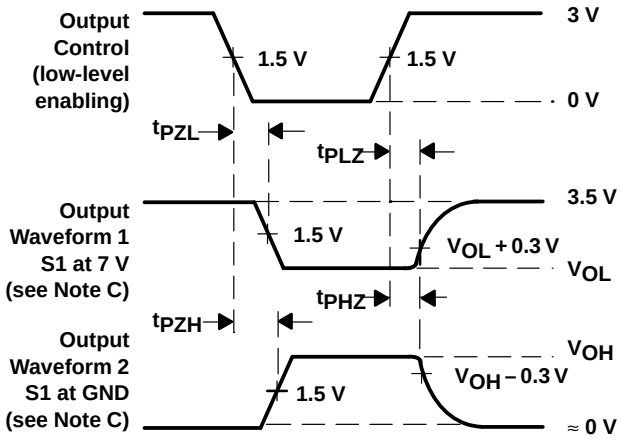
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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