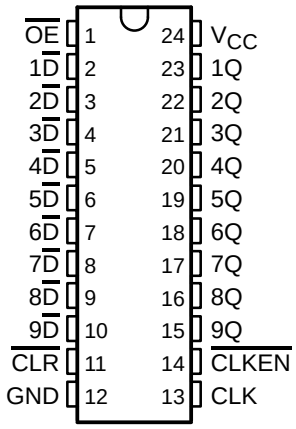
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

This 9-bit bus-interface flip-flop features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The nine flip-flops are edge-triggered D-type flip-flops. With the clock-enable ($\overline{CLKEN}$) input low, the flip-flops store data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high disables the clock buffer, thus latching the outputs. The SN74BCT29824 has inverting data ($\overline{D}$) inputs. Taking the clear ($\overline{CLR}$) input low causes the nine Q outputs to go low independent of the clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable ($\overline{OE}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT29824 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each flip-flop)

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

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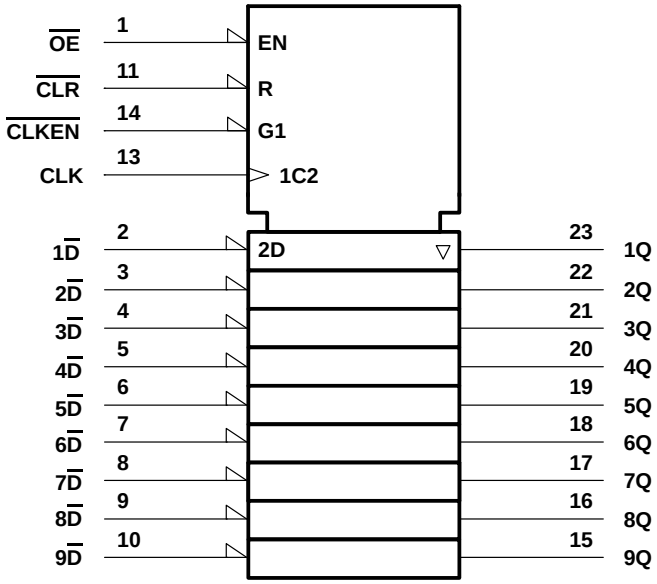
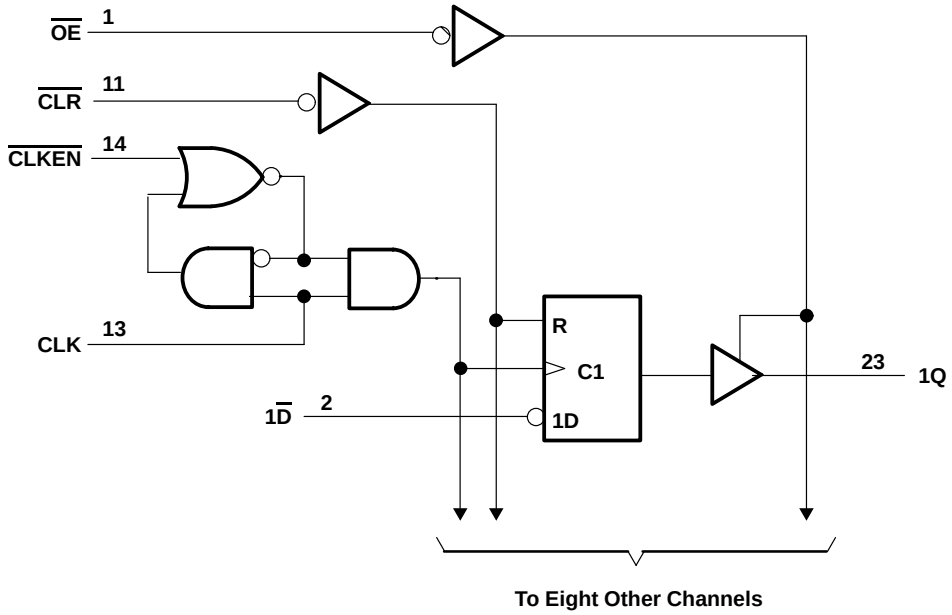
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0) . . . . . –30 mA
Current into any output in the low state, I_O . . . . . 96 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = –15 mA	2.4	3.2		V
		I_{OH} = –24 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V	–10		–75	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			–0.2	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	–75		–250	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			–20	µA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		25	35	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		6	10	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		2	6	mA
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		5.5		pF
C_o	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		7		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	125	0	125	MHz
t_w	Pulse duration	$\overline{CLR}$ low	6		6		ns
		CLK high or low	7		7		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	2		2		ns
		Data high or low	7		7		
		$\overline{CLKEN}$ high	6		6		
		$\overline{CLKEN}$ low	8		8		
t_h	Hold time after CLK↑	Data high or low	1		1		ns
		$\overline{CLKEN}$ high or low	0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			125			125		MHz
t_{PLH}	CLK	Q						ns
t_{PHL}								
t_{PHL}	$\overline{CLR}$	Q						ns
t_{PZH}	$\overline{OE}$	Q						ns
t_{PZL}								
t_{PHZ}	$\overline{OE}$	Q						ns
t_{PLZ}								

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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