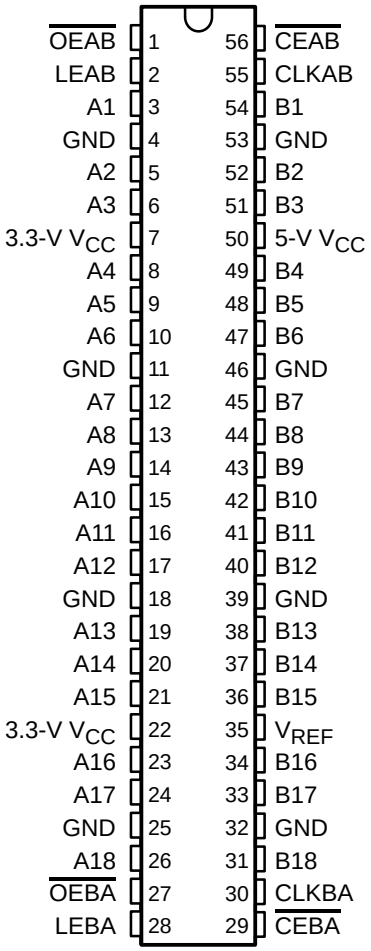
- **Translates Between GTL Signal Levels and LVCMOS, LVTTL, or 5-V TTL Signal Levels**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation on A Port (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **State-of-the-Art BiCMOS Design for Low-Static Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops With Qualified Storage Enable**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

The B port operates at GTL levels while the A port and control pins are compatible with LVCMOS, LVTTL, or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the chip-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16611 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVT16611 is characterized for operation from 0°C to 70°C.

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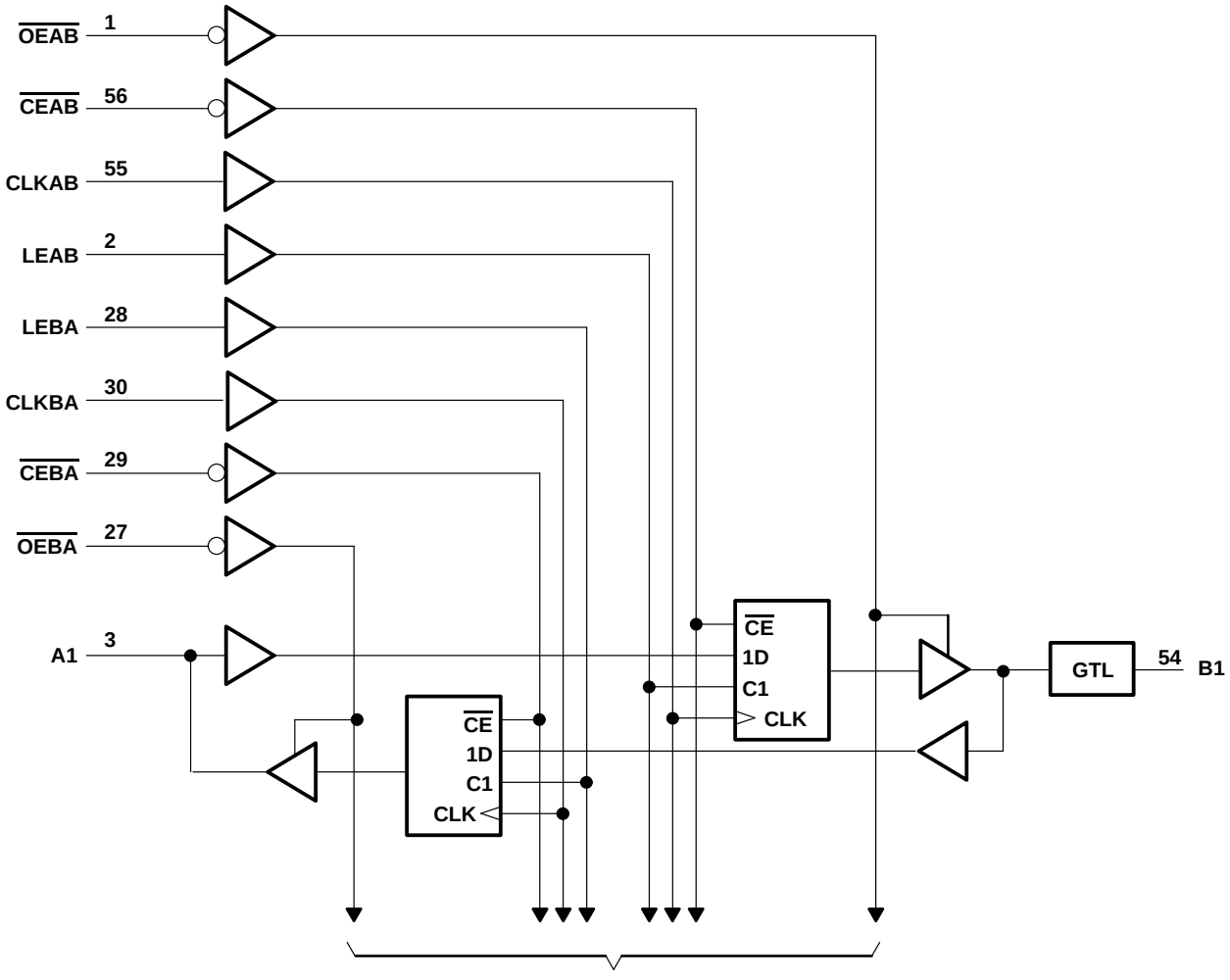
FUNCTION TABLE†

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0‡	
L	L	L	L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CEBA}$.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.
§ Output level before the indicated steady-state input conditions were established.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, 3.3-V V_{CC} . . . . . –0.5 V to 4.6 V
Supply voltage range, 5-V V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) . . . . –0.5 V to 7 V
Current into any A-port output in the low state, I_O . . . . . 128 mA
Current into any B-port output in the low state, I_O . . . . . 80 mA
Current into any A-port output in the high state, I_O (see Note 2) . . . . . 64 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package . . . . . 1 W
DL package . . . . . 1 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, 3.3 V		3.15	3.3	3.45	V
	Supply voltage, 5 V		4.75	5	5.25	
V_{REF}	Supply voltage			0.8		V
V_I	Input voltage	B port			V_{CC}	V
		Except B port			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} +50 mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF} –50 mV	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–32	mA
I_{OL}	Low-level output current	A port‡			64	mA
		B port			40	
T_A	Operating free-air temperature		0		70	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

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electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA	V_{CC} – 0.2			V
		V_{CC} = 3.15 V	I_{OH} = – 8 mA	2.4			
			I_{OH} = – 32 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	V
			I_{OL} = 16 mA			0.4	
			I_{OL} = 32 mA			0.5	
			I_{OL} = 64 mA			0.55	
	B port	V_{CC} = 3.15 V,	I_{OL} = 40 mA			0.4	
I_I	Control pins	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10	µA
	A port§	V_{CC} = 3.45 V	V_I = 5.5 V			20	µA
			V_I = V_{CC}			1	
			V_I = 0			–5	
	B port	V_{CC} = 3.45 V	V_I = V_{CC}			5	
			V_I = 0			–5	
I_{off}	A port	V_{CC} = 0	V_I or V_O = 0 to 4.5 V			100	µA
	B port		V_I or V_O = 0 to 1.2 V			100	
$I_{I(hold)}$	A port	V_{CC} = 3.15 V	V_I = 0.8 V	75			µA
			V_I = 2 V	–75			
I_{OZH}	A port	V_{CC} = 3.45 V	V_O = 3 V			1	µA
	B port		V_O = 1.2 V			10	
I_{OZL}	A port	V_{CC} = 3.45 V	V_O = 0.5 V			–1	µA
	B port		V_O = 0.4 V			–10	
I_{CC}	A port to B port	V_{CC} = 3.45 V, V_I = V_{CC} or GND	I_O = 0,				mA
	B port to A port						
	Outputs disabled						
ΔI_{CC}¶		V_{CC} = 3.45 V, A or control inputs at V_{CC} or GND	One input at 2.7 V,			1	mA
C_i	Control pins	V_I = 3.15 V or 0			4		pF
C_{io}	A port	V_O = 3.15 V or 0			10		pF
C_{io}	B port	Per IEEE1194.0-1991				5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	150	MHz
t_w	Pulse duration	LEAB or LEBA high			ns
		CLKAB or CLKBA high or low			
t_{su}	Setup time	A before CLKAB↑	1.5		ns
		B before CLKAB↑	3		
		A before LEAB↓	0.5		
		B before LEBA↓	1.5		
		$\overline{CEAB}$ before CLKAB↑			
		$\overline{CEBA}$ before CLKBA↑			
		$\overline{CEAB}$ before LEAB↓			
		$\overline{CEBA}$ before LEBA↓			
t_h	Hold time	A after CLKAB↑	1		ns
		B after CLKAB↑	0		
		A after LEAB↓	2.5		
		B after LEBA↓	2		
		$\overline{CEAB}$ after CLKAB↑			
		$\overline{CEBA}$ after CLKBA↑			
		$\overline{CEAB}$ after LEAB↓			
		$\overline{CEBA}$ after LEBA↓			

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}						MHz
t_{PLH}	A	B			3.2	ns
t_{PHL}					3.2	
t_{PLH}	LEAB	B			4	ns
t_{PHL}					4	
t_{PLH}	CLKAB	B			4.3	ns
t_{PHL}					4.3	
t_{PLH}	$\overline{OEAB}$	B			4.5	ns
t_{PHL}					4.5	
t_f	Transition time, B outputs (0.5 V to 1 V)			1.7		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.6		ns
t_{PLH}	B	A			6.5	ns
t_{PHL}					6.5	
t_{PLH}	LEBA	A			6.3	ns
t_{PHL}					6.3	
t_{PLH}	CLKBA	A			6.3	ns
t_{PHL}					6.3	
t_{EN}	$\overline{OEBA}$	A			5.5	ns
t_{DIS}					6	

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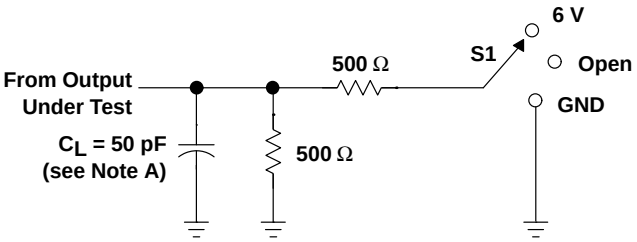
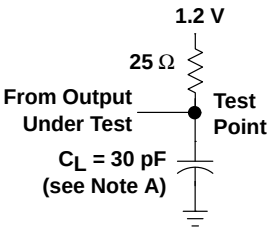
PARAMETER MEASUREMENT INFORMATION

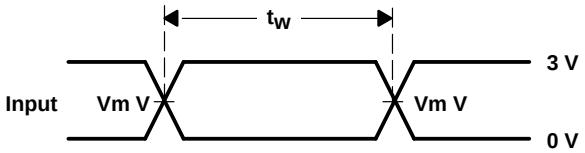


LOAD CIRCUIT FOR A OUTPUTS

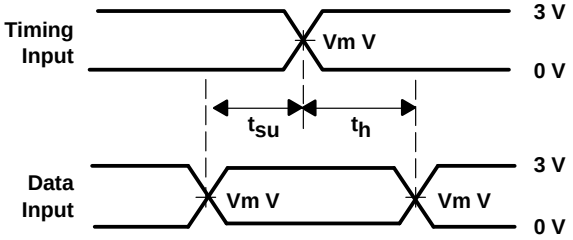


LOAD CIRCUIT FOR B OUTPUTS

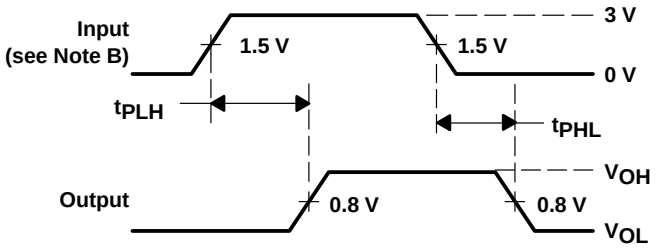
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



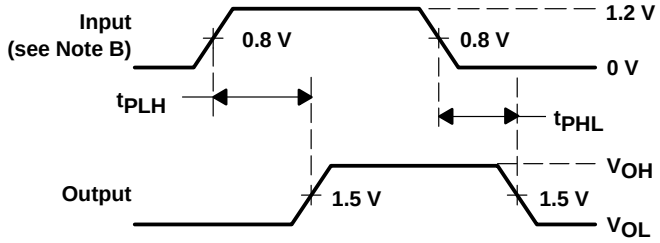
VOLTAGE WAVEFORMS
PULSE DURATION
(Vm = 1.5 V for A port and 0.8 V for B port)



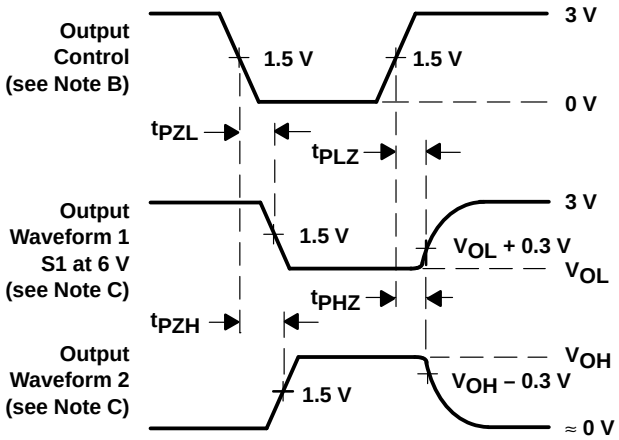
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(Vm = 1.5 V for A port and 0.8 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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