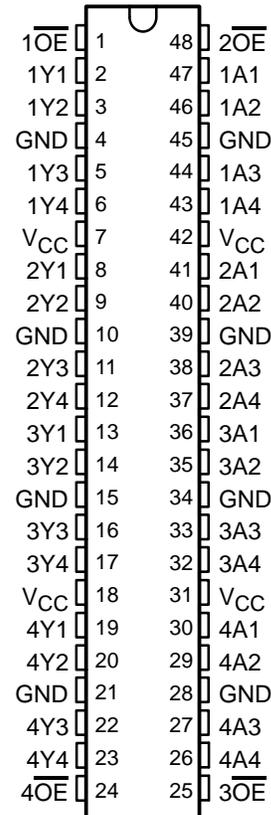


SN54LVTH162244, SN74LVTH162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- Output Ports Have Equivalent 22- Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*[™] Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Inputs/Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH162244 . . . WD PACKAGE
SN74LVTH162244 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVTH162244 are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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SN54LVTH162244, SN74LVTH162244

3.3-V ABT 16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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description (continued)

The outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVTH162244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN54LVTH162244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH162244 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 4-bit buffer)

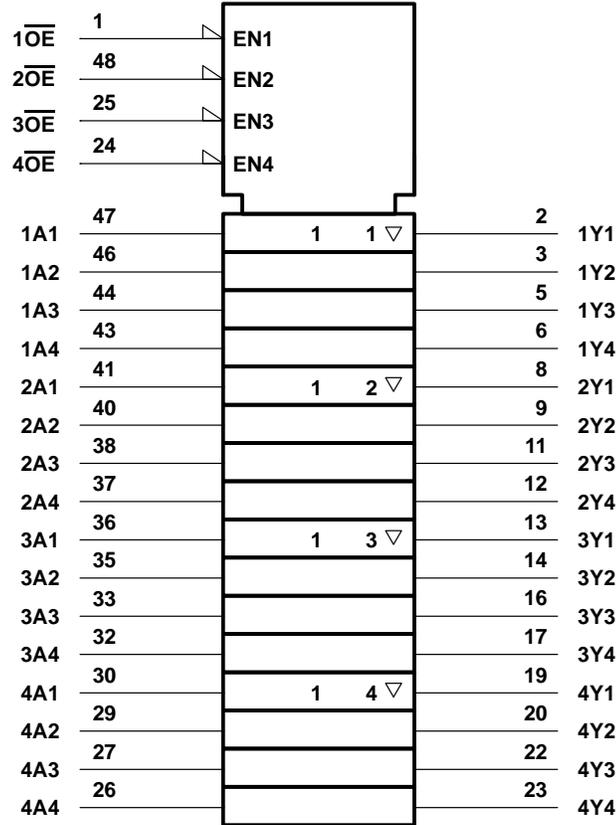
INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z



SN54LVTH162244, SN74LVTH162244
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WITH 3-STATE OUTPUTS

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logic symbol†

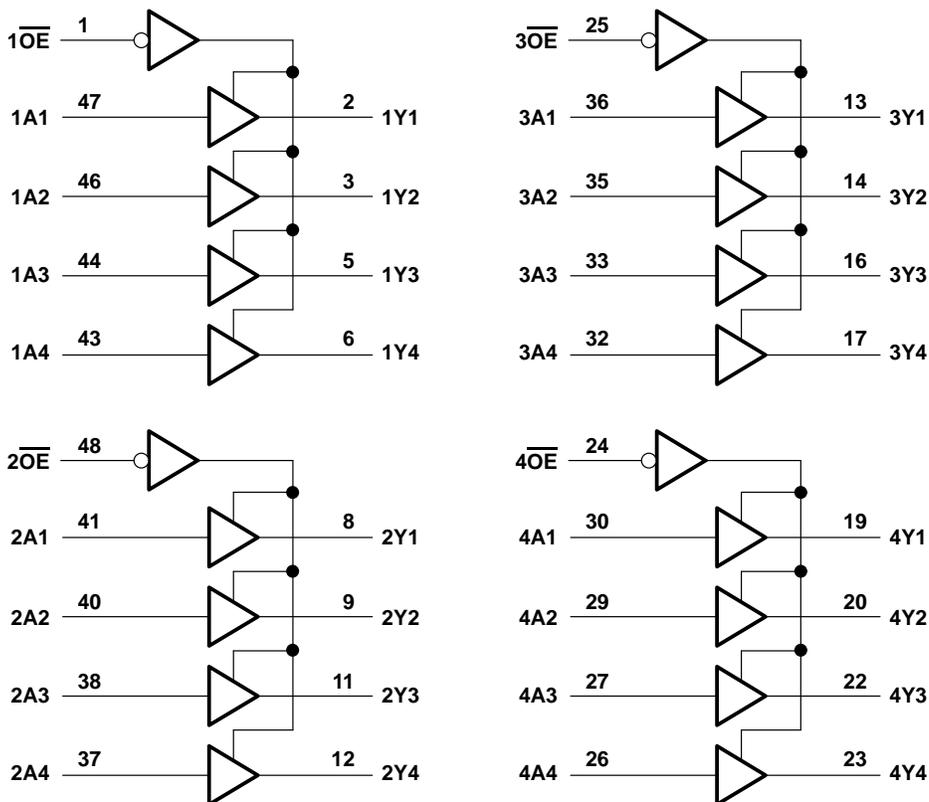


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVTH162244, SN74LVTH162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_{OL}	30 mA
Current into any output in the high state, I_{OH} (see Note 2)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.



SN54LVTH162244, SN74LVTH162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		SN54LVTH162244		SN74LVTH162244		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-12		-12	mA
I _{OL}	Low-level output current		12		12	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled			10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH162244		SN74LVTH162244		UNIT	
				MIN	TYP†	MAX	MIN		TYP†
V _{IK}		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2		V	
V _{OH}		V _{CC} = 3 V,	I _{OH} = -12 mA	2		2		V	
V _{OL}		V _{CC} = 3 V,	I _{OL} = 12 mA			0.8		V	
I _I		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V			10		μA	
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1			
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}			1			
			V _I = 0			-5			
I _{off}		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V					±100	
I _I (hold)	A inputs	V _{CC} = 3 V	V _I = 0.8 V	75		75		μA	
			V _I = 2 V	-75		-75			
I _{OZH}		V _{CC} = 3.6 V,	V _O = 3 V			5		μA	
I _{OZL}		V _{CC} = 3.6 V,	V _O = 0.5 V			-5		μA	
I _{OZPU} ‡		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, \overline{OE} = X				±100		μA	
I _{OZPD} ‡		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, \overline{OE} = X				±100		μA	
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			0.19		mA	
			Outputs low			5			
			Outputs disabled			0.19			0.19
ΔI _{CC} §		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				0.2		0.2	mA
C _i		V _I = 3 V or 0				4		4	pF
C _o		V _O = 3 V or 0				9		9	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This parameter is characterized but not production tested.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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WITH 3-STATE OUTPUTS

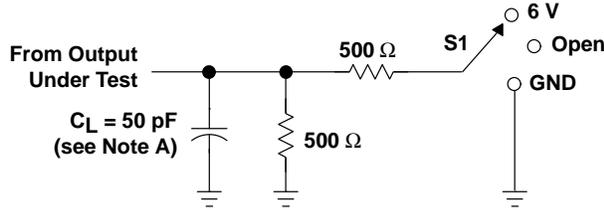
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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162244				SN74LVTH162244				UNIT	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t_{PLH}	A	Y	1.3	4.5		5.1	1.4	3.4	4		4.8	ns
t_{PHL}			1.1	3.9		4.5	1.2	2.9	3.6		4.1	
t_{PZH}	\overline{OE}	Y	1.1	5.3		6.7	1.2	3.9	5.1		6.5	ns
t_{PZL}			1.3	4.7		6.1	1.4	3.8	4.5		5.8	
t_{PHZ}	\overline{OE}	Y	2.1	5.3		5.6	2.2	4.4	5		5.4	ns
t_{PLZ}			1.9	5.5		5.8	2	4.2	5		5.4	
$t_{sk(o)}$								0.5			ns	

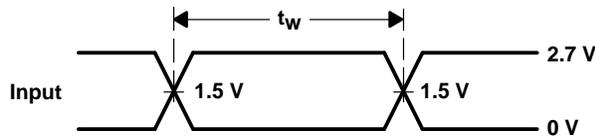
† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

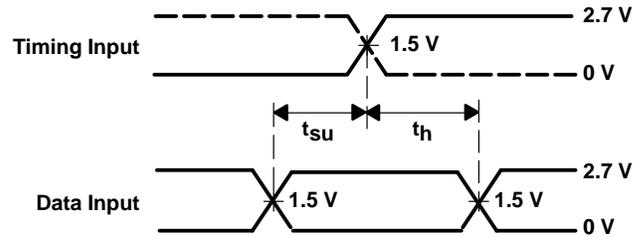


LOAD CIRCUIT

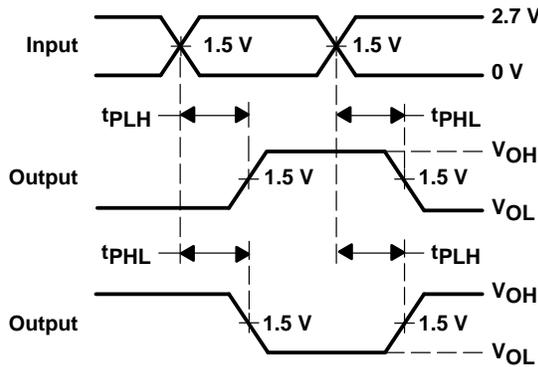
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



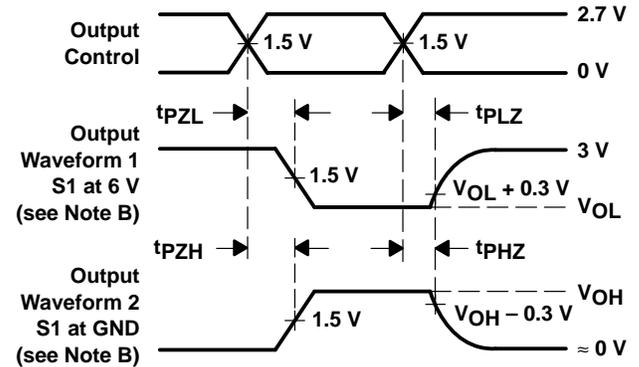
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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