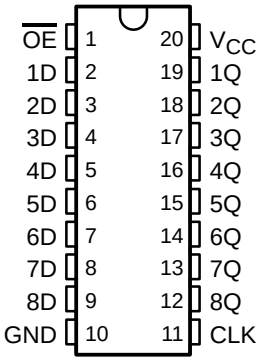
- **State-of-the-Art BiCMOS Design Significantly Reduces $I_{CCZ}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (N)**

**DW OR N PACKAGE**
**(TOP VIEW)**




## description

This octal edge-triggered D-type flip-flop features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs will be set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable ($\overline{OE}$) does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

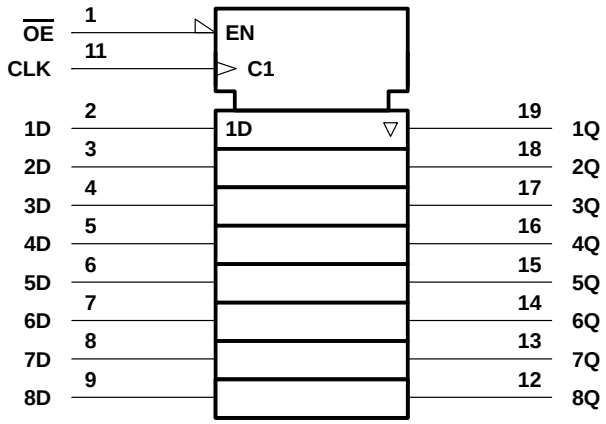
The outputs, which are designed to source or sink up to 12 mA, include 33-Ω series resistors to reduce overshoot and undershoot.

The SN74BCT2574 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each flip-flop)**

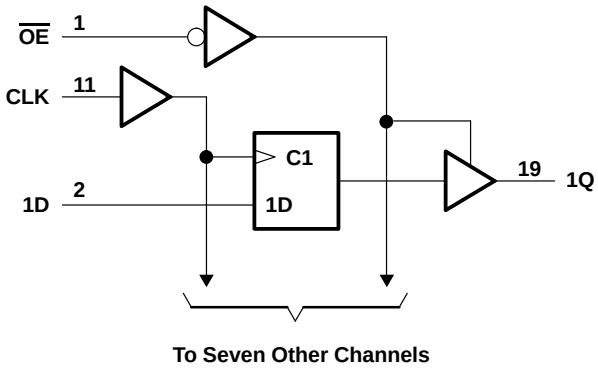
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†

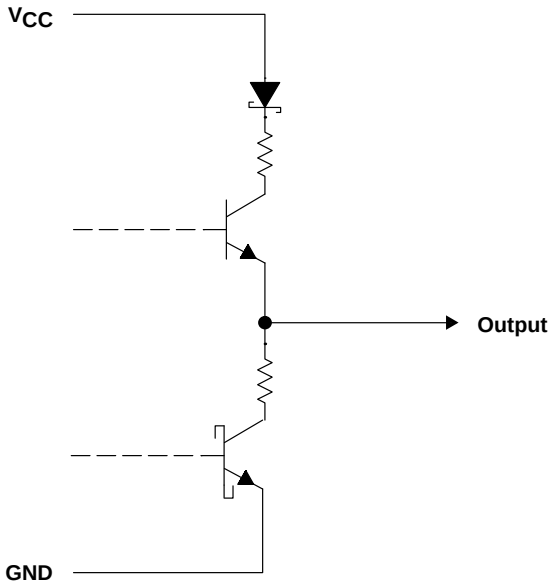



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## schematic of each output



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$ . . . . . –0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –30 mA
Current into any output in the low state, $I_O$ . . . . . 60 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions (see Note 2)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High-level output current | | | –12 | mA |
| $I_{OL}$ | Low-level output current | | | 12 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

NOTE 2: Unused or floating inputs must be held high or low.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 1 mA | 2.4 | | | V |
| | | $I_{OH}$ = –12 mA | 2 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 1 mA | | 0.15 | 0.5 | V |
| | | $I_{OL}$ = 12 mA | | 0.35 | 0.8 | |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | | 0.4 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | –0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | –100 | | –225 | mA |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | µA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | Outputs open | | 36 | 58 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | Outputs open | | 2 | 6 | mA |
| $I_{CCZ}$ | $V_{CC}$ = 5.5 V, | Outputs open | | 2 | 8 | mA |
| $C_i$ | $V_{CC}$ = 5 V, | $V_I$ = 2.5 V or 0.5 V | | 4.5 | | pF |
| $C_o$ | $V_{CC}$ = 5 V, | $V_O$ = 2.5 V or 0.5 V | | 9 | | pF |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | | 0 | 83 | 0 | 83 | MHz |
| $t_w$ | Pulse duration, CLK high or low | | 6 | | 6 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | High | 5 | | 5 | | ns |
| | | Low | 6 | | 6 | | |
| $t_h$ | Hold time, data after CLK↑ | High or low | 0 | | 0 | | ns |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Note 3)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | 83 | | | 83 | | MHz |
| $t_{PLH}$ | CLK | Q | 2.1 | 6.1 | 8 | 2.1 | 9.5 | ns |
| $t_{PHL}$ | | | 2.8 | 6.1 | 8.2 | 2.8 | 8.8 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | 2.8 | 6.2 | 8.1 | 2.8 | 9.8 | ns |
| $t_{PZL}$ | | | 4.2 | 7.5 | 9.3 | 4.2 | 10.9 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 1.1 | 3.7 | 5.3 | 1.1 | 5.9 | ns |
| $t_{PLZ}$ | | | 1.6 | 4.1 | 5.8 | 1.6 | 6.3 | |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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