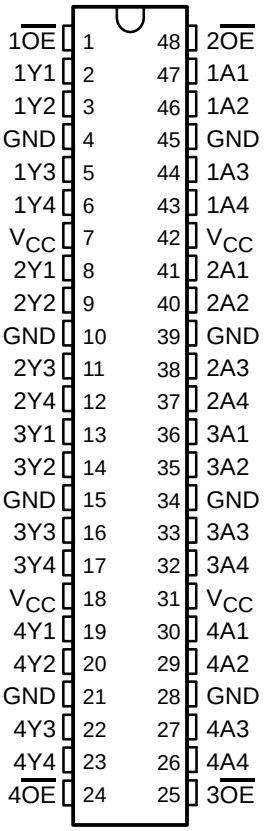
- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162240 . . . WD PACKAGE
SN74ABT162240 . . . DL PACKAGE
(TOP VIEW)



description

The ′ABT162240 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162240 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT162240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

PRODUCT PREVIEW

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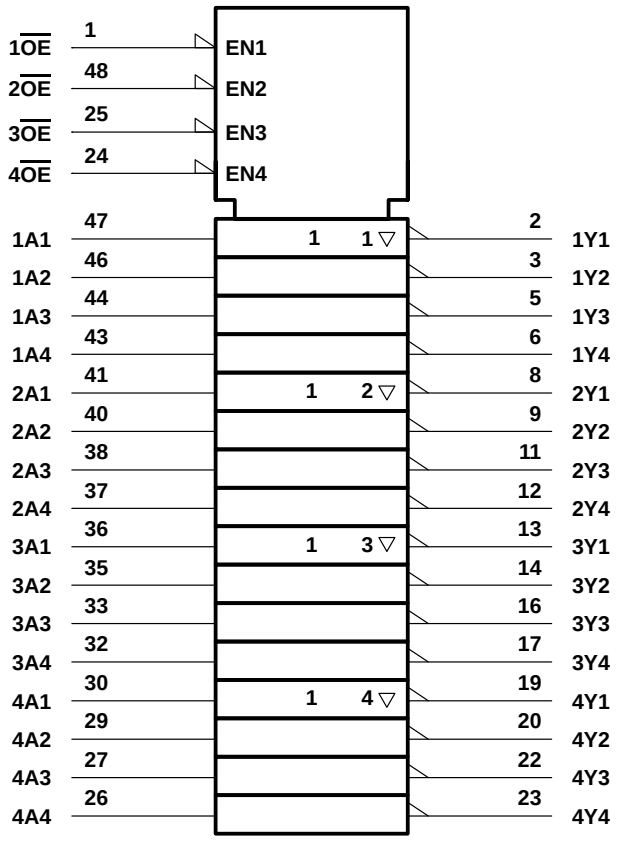
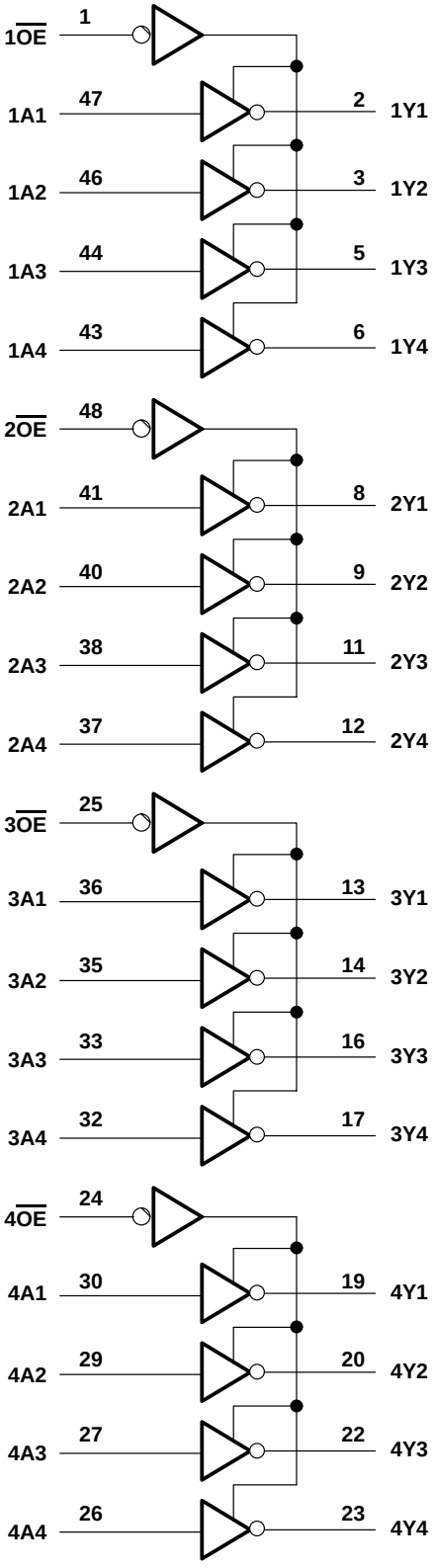
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 30 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) . . . . . 0.85 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162240		SN74ABT162240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–12		–12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

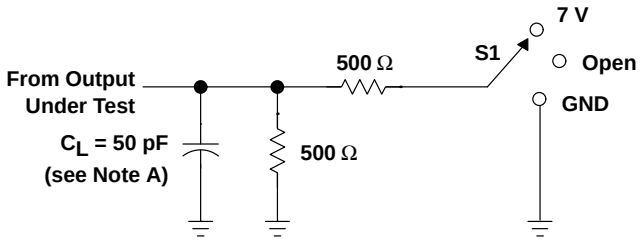
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT162240		SN74ABT162240		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 1 mA			3.35			3.3		3.35		V
	V_{CC} = 5 V, I_{OH} = – 1 mA			3.85			3.8		3.85		
	V_{CC} = 4.5 V, I_{OH} = – 3 mA			3.1			3		3.1		
	V_{CC} = 4.5 V, I_{OH} = – 12 mA			2.6‡					2.6		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA				0.4	0.8		0.8		0.65	V
	V_{CC} = 4.5 V, I_{OL} = 12 mA									0.8	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND					±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V					–50		–50		–50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				7						pF
C_o	V_O = 2.5 V or 0.5 V				7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

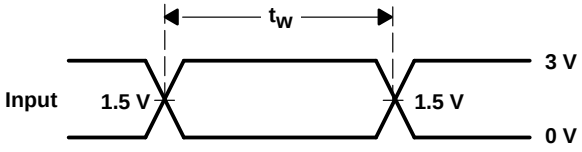
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

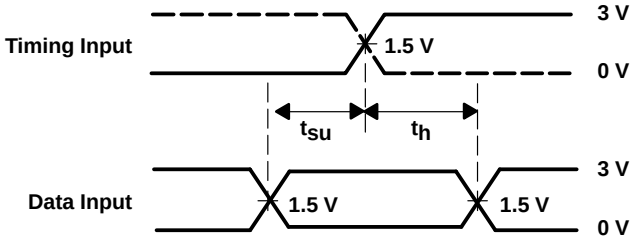


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

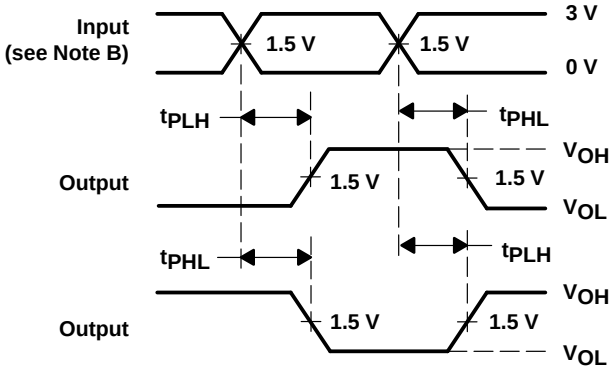
LOAD CIRCUIT FOR OUTPUTS



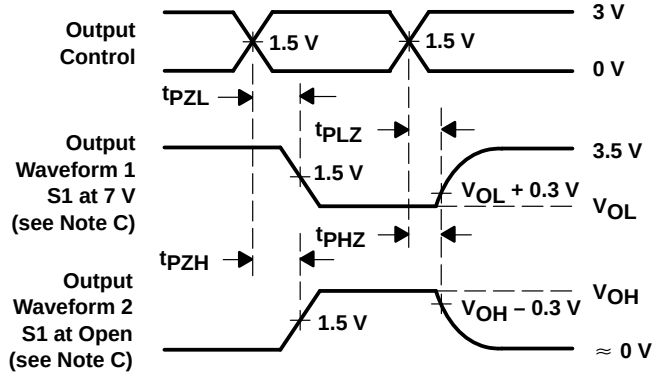
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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