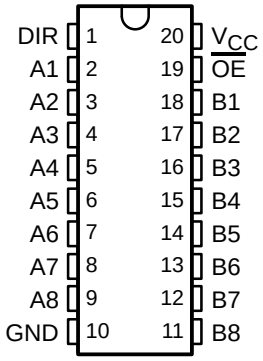
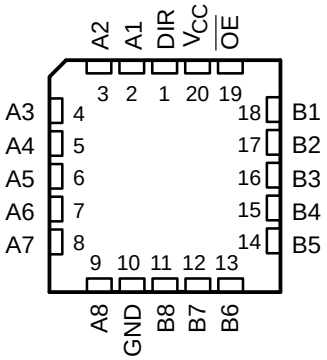
- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package**

**SN54ABT2245 . . . J OR W PACKAGE**
**SN74ABT2245 . . . DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54ABT2245 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal transceivers and line drivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The B-port outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

When $V_{CC}$ is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54ABT2245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT2245 is characterized for operation from –40°C to 85°C.

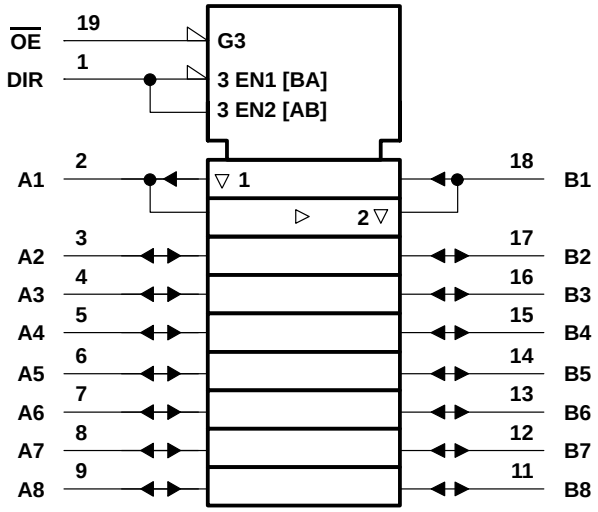
**FUNCTION TABLE**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

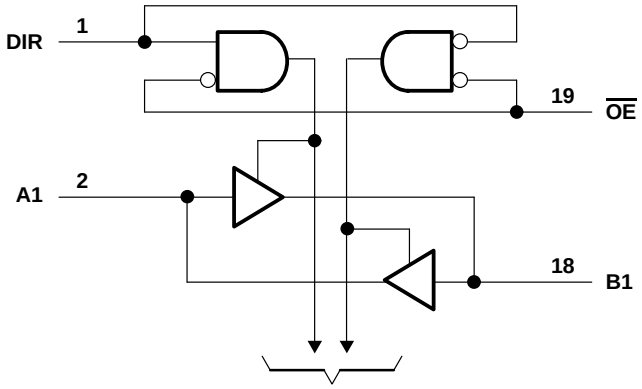
EPIC-IIB is a trademark of Texas Instruments Incorporated.

## logic symbol†

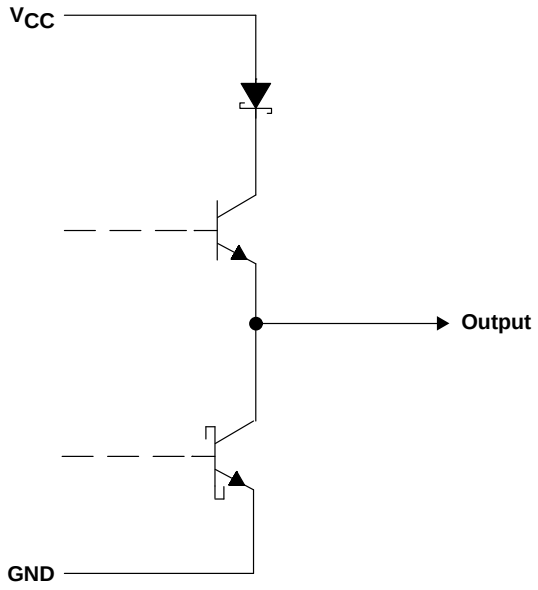



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

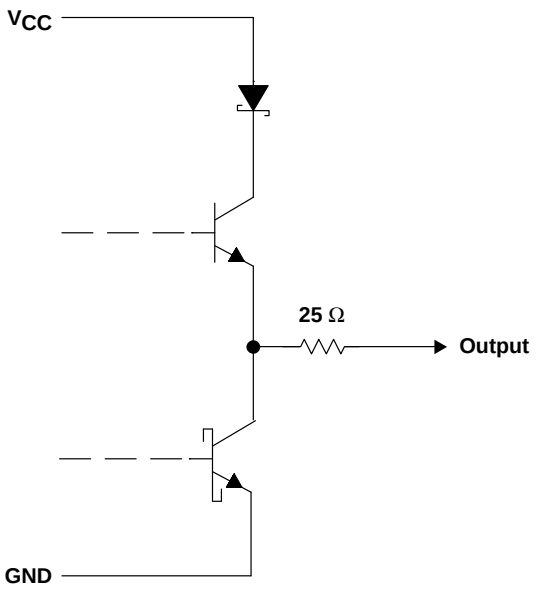
## logic diagram (positive logic)



**schematic of A-port outputs**




**schematic of B-port outputs**




All resistor values shown are nominal.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | | |
|---|---|---|
| Supply voltage range, $V_{CC}$ | | –0.5 V to 7 V |
| Input voltage range, $V_I$ (except I/O ports) (see Note 1) | | –0.5 V to 7 V |
| Voltage range applied to any output in the high or power-off state, $V_O$ | | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$: | SN54ABT2245 (except B port) | 96 mA |
| | SN74ABT2245 (except B port) | 128 mA |
| | B port | 30 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | | –18 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | | –50 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): | DB package | 115°C/W |
| | DW package | 97°C/W |
| | N package | 67°C/W |
| | PW package | 128°C/W |
| Storage temperature range, $T_{stg}$ | | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54ABT2245 | | SN74ABT2245 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | A port | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port | | 48 | | 64 | mA |
| | | B port | | 12 | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 5 | | 5 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | 200 | | 200 | | μs/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

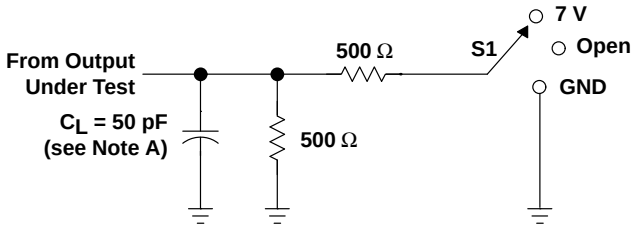
| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABT2245 | | SN74ABT2245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | B port | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –1 mA | 3.35 | | | 3.3 | | 3.35 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –1 mA | 3.85 | | | 3.8 | | 3.85 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | | | | 3 | | 3.1 | | |
| | | | $I_{OH}$ = –12 mA | 2.6 | | | | | 2.6 | | |
| | A port | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | 2.5 | | |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | | | | | 2 | | |
| $V_{OL}$ | B port | $V_{CC}$ = 4.5 V | $I_{OL}$ = 8 mA | | | 0.65 | | 0.8 | | 0.65 | V |
| | | | $I_{OL}$ = 12 mA | | | 0.8 | | | | 0.8 | |
| | A port | | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| $V_{hys}$ | | | | | 100 | | | | | | mV |
| $I_I$ | Control inputs | $V_{CC}$ = 0 to 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 2.1 V to 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±20 | | ±20 | | ±20 | |
| $I_{OZH}$‡ | | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 2.7 V, $\overline{OE}$ ≥ 2 V | | | | 10 | | 10 | | 10 | µA |
| $I_{OZL}$‡ | | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 0.5 V, $\overline{OE}$ ≥ 2 V | | | | –10 | | –10 | | –10 | µA |
| $I_{OZPU}$§ | | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 0.5 V to 2.7 V, $\overline{OE}$ = X | | | | ±50 | | ±50 | | ±50 | µA |
| $I_{OZPD}$§ | | $V_{CC}$ = 2.1 V to 0, $V_O$ = 0.5 V to 2.7 V, $\overline{OE}$ = X | | | | ±50 | | ±50 | | ±50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | | 50 | µA |
| $I_O$¶ | B port | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –25 | | –100 | –25 | –100 | –25 | –100 | mA |
| | A port | | | –50 | –100 | –180 | –50 | –180 | –50 | –180 | |
| $I_{CC}$ | A or B ports | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 1 | 250 | | 250 | | 250 | µA |
| | | | Outputs low | | 24 | 32 | | 32 | | 32 | mA |
| | | | Outputs disabled | | 0.5 | 250 | | 250 | | 250 | µA |
| $\Delta I_{CC}$# | Data inputs | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | Outputs enabled | | | 1.5 | | 1.5 | | 1.5 | mA |
| | | | Outputs disabled | | | 0.05 | | 0.05 | | 0.05 | |
| | Control inputs | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | |
| $C_i$ | | $V_I$ = 2.5 V or 0.5 V | | | 3 | | | | | | pF |
| $C_{io}$ | | $V_O$ = 2.5 V or 0.5 V | | | 6 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ This parameter is characterized but not production tested.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

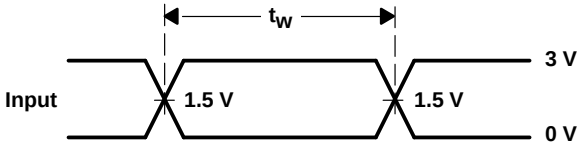
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT2245 | | SN74ABT2245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | B | 1 | 2.5 | 3.4 | 1 | 4 | 1 | 3.8 | ns |
| $t_{PHL}$ | | | 1 | 3.2 | 4.2 | 1 | 4.6 | 1 | 4.5 | |
| $t_{PLH}$ | B | A | 1 | 2.2 | 3.2 | 1 | 3.8 | 1 | 3.6 | ns |
| $t_{PHL}$ | | | 1 | 2.7 | 3.6 | 1 | 4.2 | 1 | 4 | |
| $t_{PZH}$ | $\overline{OE}$ | A | 1 | 3.3 | 4.6 | 1 | 5.6 | 1 | 5.5 | ns |
| $t_{PZL}$ | | | 1 | 3.2 | 4.7 | 1 | 6 | 1 | 5.7 | |
| $t_{PHZ}$ | $\overline{OE}$ | A | 2 | 4 | 5.1 | 2 | 5.7 | 2 | 5.6 | ns |
| $t_{PLZ}$ | | | 1 | 2.9 | 4 | 1 | 4.6 | 1 | 4.5 | |
| $t_{PZH}$ | $\overline{OE}$ | B | 1.5 | 3.6 | 4.9 | 1.5 | 6.3 | 1.5 | 6.1 | ns |
| $t_{PZL}$ | | | 1.5 | 3.9 | 5.3 | 1.5 | 6.6 | 1.5 | 6.3 | |
| $t_{PHZ}$ | $\overline{OE}$ | B | 1.5 | 3.6 | 4.7 | 1.5 | 5.5 | 1.5 | 5.3 | ns |
| $t_{PLZ}$ | | | 1.5 | 3.3 | 4.4 | 1.5 | 4.9 | 1.5 | 4.8 | |

## PARAMETER MEASUREMENT INFORMATION

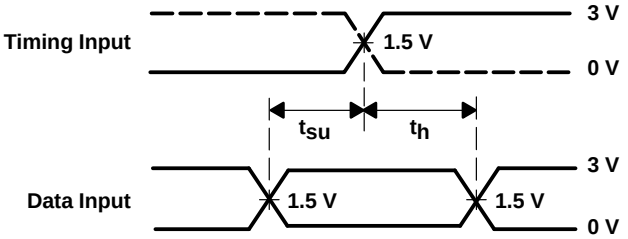



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

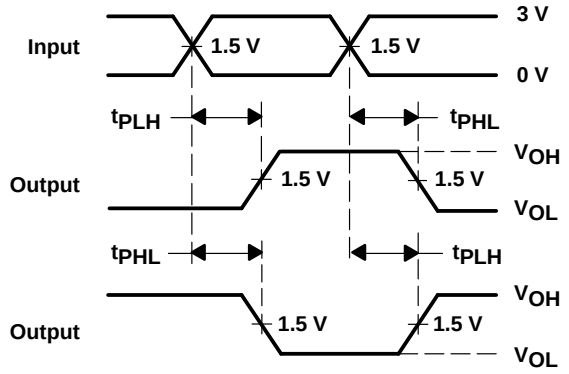
LOAD CIRCUIT



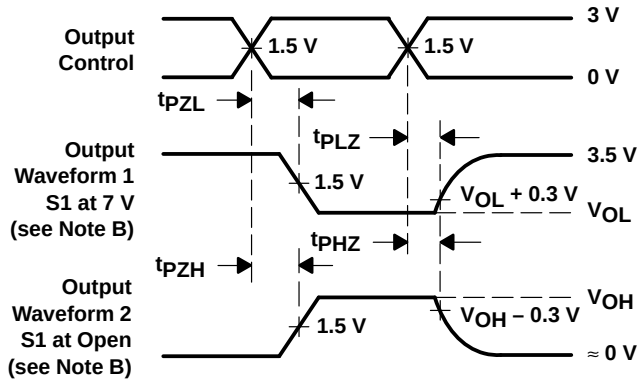

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.