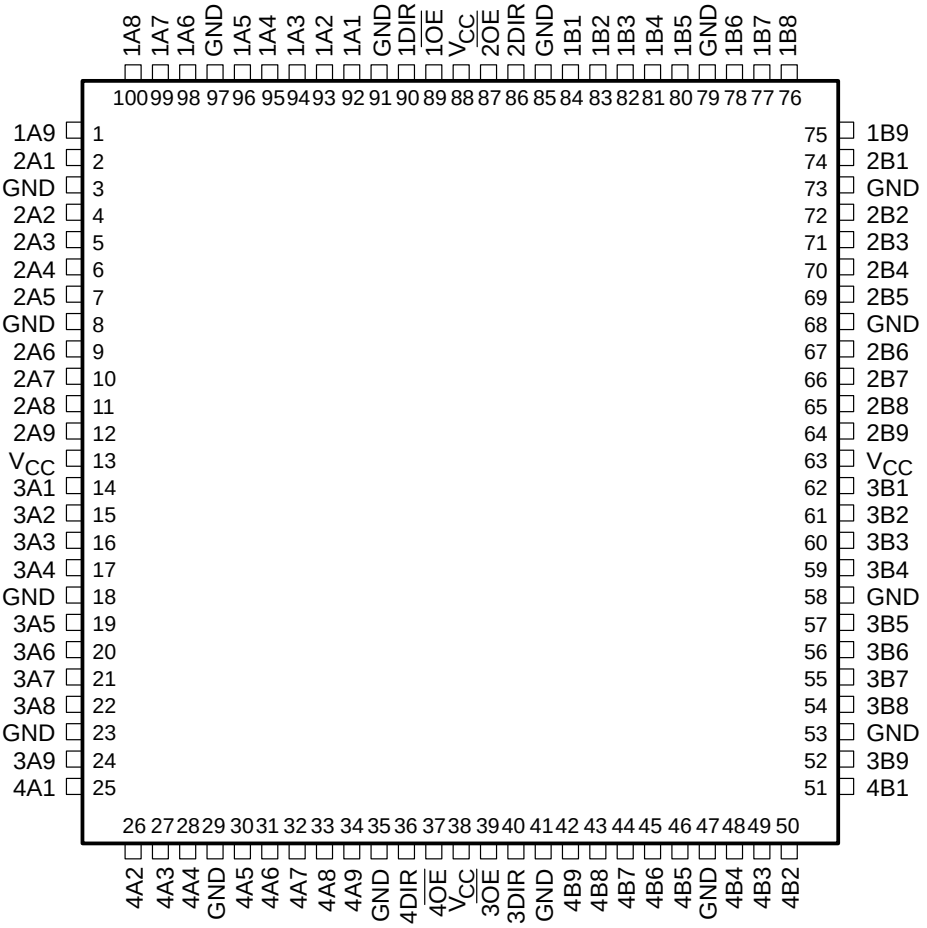
- **Members of the Texas Instruments *Widebus+*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Released as DSCC SMD 5962-9557701NXD**
- **PZ Package Qualified for Military Per MIL-PRF-38535 (QML)**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include 100-Pin Plastic Thin Quad Flat (PZ) Package With 14 × 14-mm Body Using 0.5-mm Lead Pitch and Space-Saving 100-Pin Ceramic Quad Flat (HS) Package†**

'ABTH32245 . . . PZ PACKAGE
(TOP VIEW)



† The HS package is not production released.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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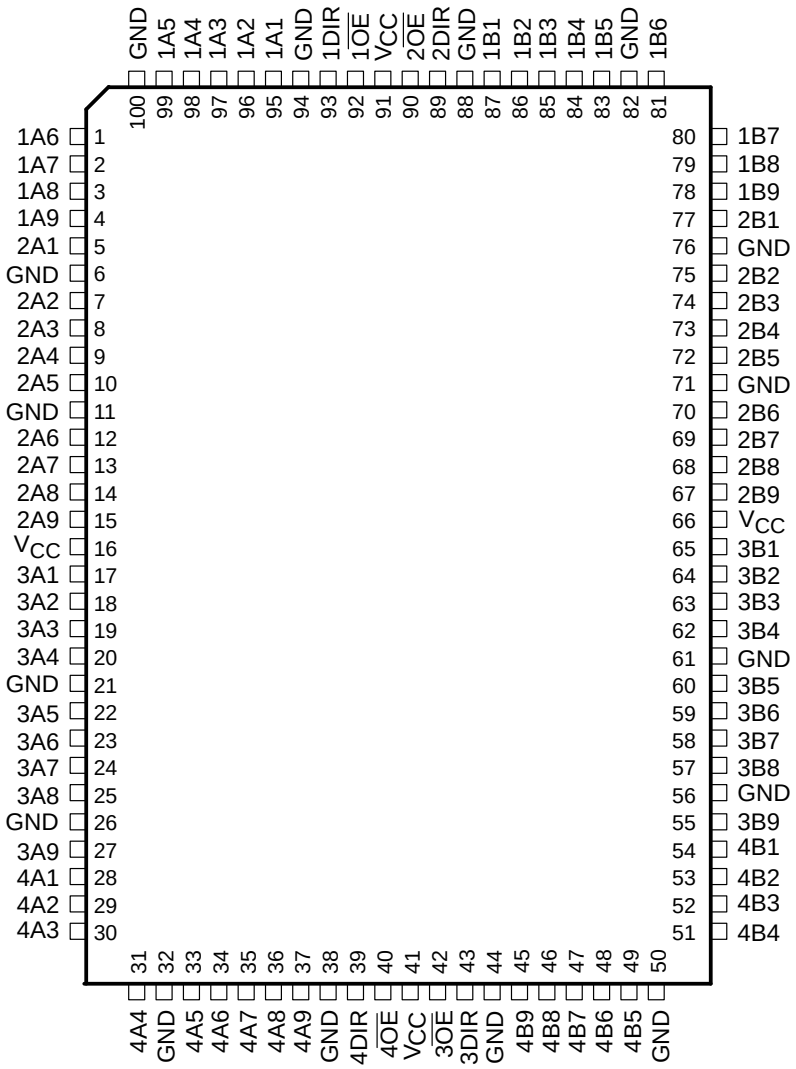
SN54ABTH32245 . . . HS PACKAGE†
(TOP VIEW)



† For HS package availability, please contact the factory or your local TI Field Sales Office.

description

The ’ABTH32245 are 36-bit (quad 9-bit) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as four 9-bit transceivers, two18-bit transceivers, or one 36-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) inputs. The output-enable ($\overline{OE}$) inputs can be used to disable the device so that the buses are effectively isolated.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

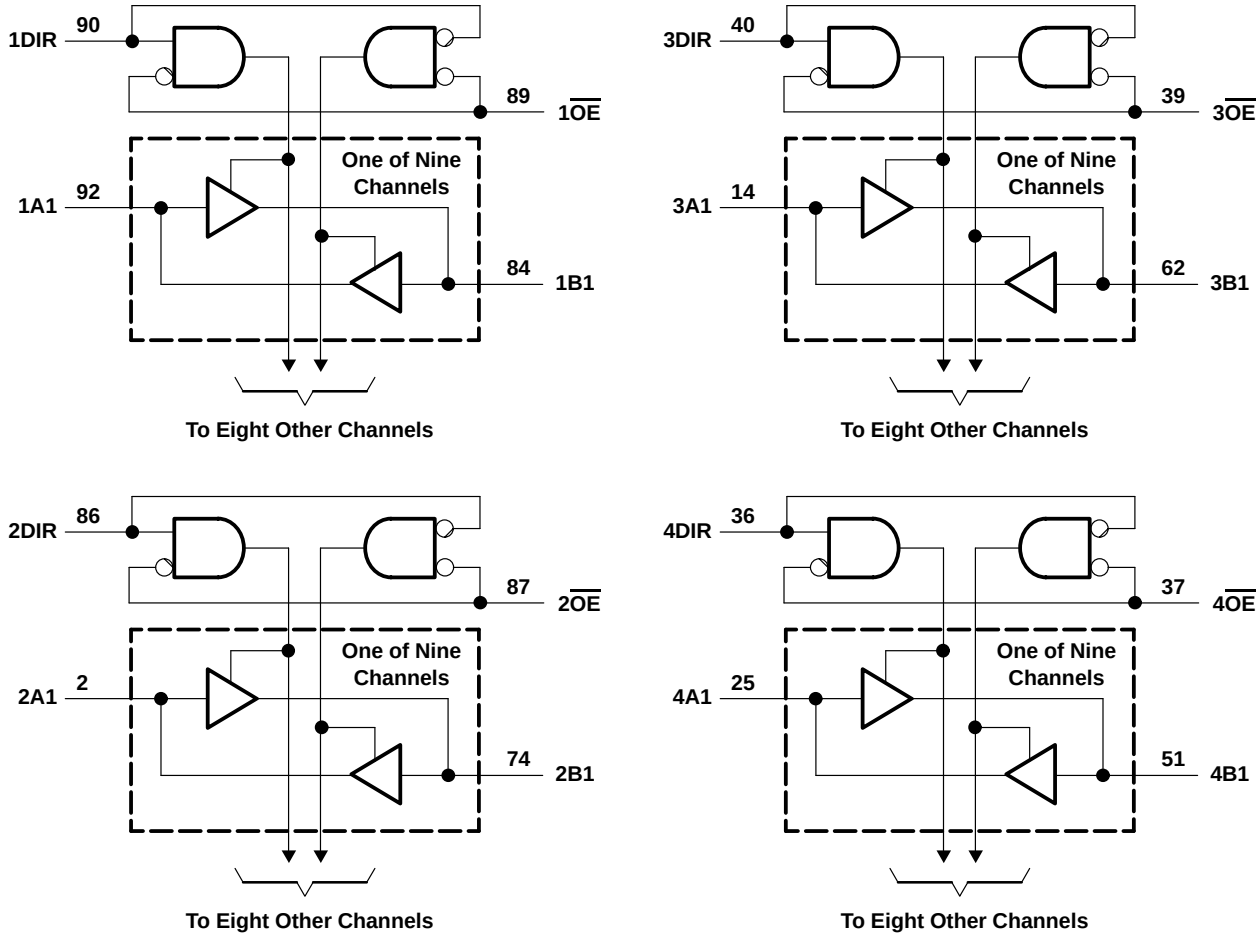
description (continued)

The SN54ABTH32245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTH32245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 9-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



Pin numbers shown are for the PZ package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABTH32245 . . . . . 96 mA
SN74ABTH32245 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): PZ package . . . . . 50°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABTH32245		SN74ABTH32245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ABTH32245			SN74ABTH32245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5			2.5			V
		V_{CC} = 5 V,	I_{OH} = –3 mA	3			3			
		V_{CC} = 4.5 V	I_{OH} = –24 mA	2						
			I_{OH} = –32 mA				2			
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55			0.55	V
			I_{OL} = 64 mA						0.55	
V_{hys}					100			100		mV
I_I	Control inputs	V_{CC} = 0 to 5.5 V,	V_I = V_{CC} or GND						±1	µA
	A or B ports	V_{CC} = 2.1 V to 5.5 V,	V_I = V_{CC} or GND						±20	
	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1				µA
	A or B ports					±20				
$I_{I(hold)}$	A or B ports	V_{CC} = 4.5 V	V_I = 0.8 V	100			100			µA
			V_I = 2 V	–100			–100			
I_{OZPU}‡		V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50			±50	µA
I_{OZPD}‡		V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50			±50	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V						±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50			50	µA
I_O§		V_{CC} = 5.5 V,	V_O = 2.5 V	–50	–100	–180	–50	–100	–180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			3			3	mA
			Outputs low			20			20	
			Outputs disabled			2			2	
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1			1	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			3.5			3.5		pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			9.5			9.5		pF

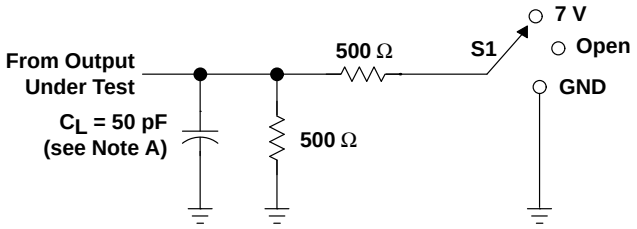
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This parameter is specified by characterization.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C#			SN54ABTH32245		SN74ABTH32245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.7	3.2	4.4	1	5.3	1.7	5	ns
t_{PHL}			1.7	3.3	4.6	1	5.3	1.7	5.2	
t_{PZH}	$\overline{OE}$	B or A	1.6	4.2	6.1	1	7.6	1.6	7.3	ns
t_{PZL}			2.7	5.2	7	1.5	8.2	2.7	8.1	
t_{PHZ}	$\overline{OE}$	B or A	1.3	3.9	6.1	0.8	6.7	1.3	6.5	ns
t_{PLZ}			2	4.4	6.6	1	7.2	2	6.9	

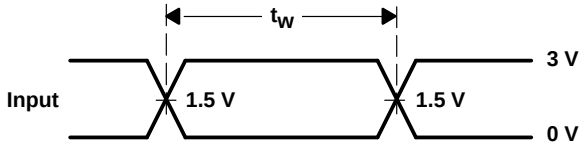
These limits apply only to the SN74ABTH32245

PARAMETER MEASUREMENT INFORMATION

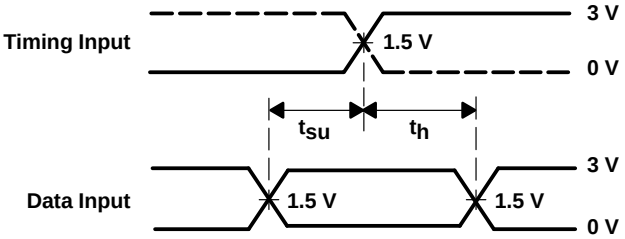


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

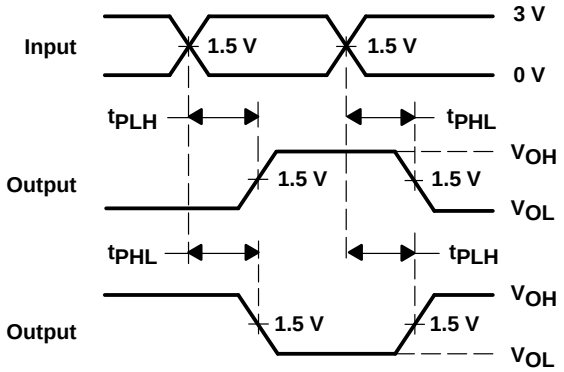
LOAD CIRCUIT



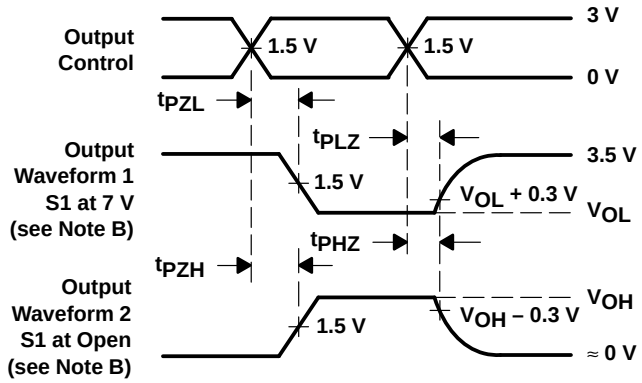
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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