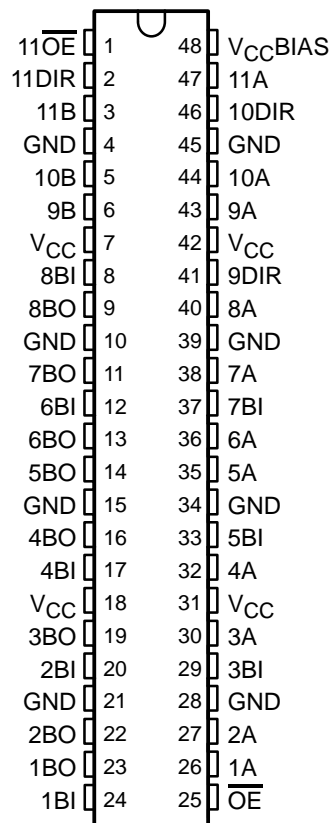


SN54ABTE16246, SN74ABTE16246 11-BIT INCIDENT-WAVE SWITCHING BUS TRANSCEIVERS WITH 3-STATE AND OPEN-COLLECTOR OUTPUTS

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- Support the VME64 ETL Specification
- Reduced TTL-Compatible Input Threshold Range
- High-Drive Outputs ($I_{OH} = -60$ mA
 $I_{OL} = 90$ mA) Support Equivalent 25- Ω Incident-Wave Switching
- V_{CCBIAS} Pin Minimizes Signal Distortion During Live Insertion
- Internal Pullup Resistor on \overline{OE} Keeps Outputs in High-Impedance State During Power Up or Power Down
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Equivalent 25- Ω Series-Damping Resistor on B Port
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin-Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABTE16246 . . . WD PACKAGE
SN74ABTE16246 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABTE16246 are 11-bit noninverting transceivers designed for asynchronous two-way communication between buses. These devices have open-collector and 3-state outputs. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated. When \overline{OE} is low, the device is active.

The B port has an equivalent 25- Ω series output resistor to reduce ringing. Active bus-hold inputs on the B port hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via V_{CCBIAS} , which establishes a voltage between 1.3 V and 1.7 V when V_{CC} is not connected.

The SN54ABTE16246 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABTE16246 is characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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WITH 3-STATE AND OPEN-COLLECTOR OUTPUTS

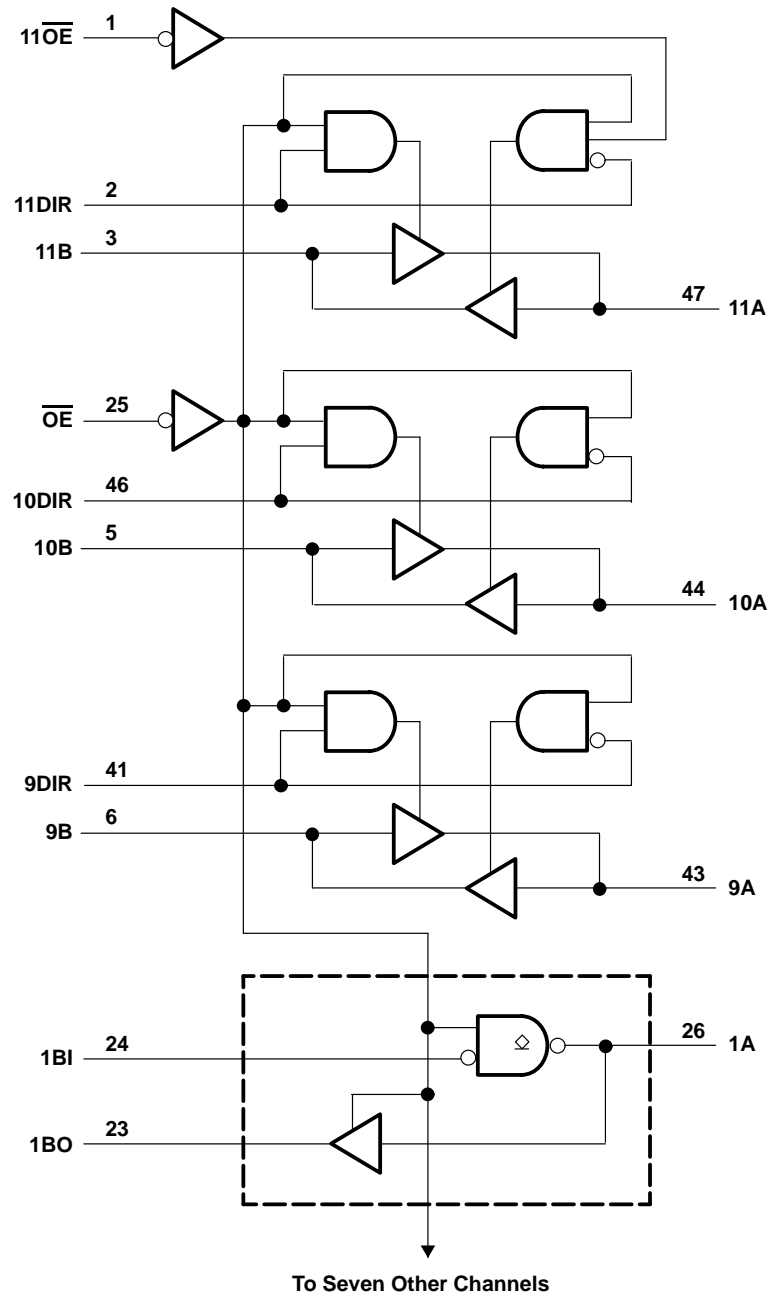
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FUNCTION TABLE

INPUTS					OPERATION
\overline{OE}	9DIR	10DIR	11DIR	11 \overline{OE}	
H	X	X	X	X	Isolation
L	X	X	X	X	1BI–8BI data to 1A–8A bus (OC [†]), 1A–8A data to 1BO–8BO bus
L	L	X	X	X	9A data to 9B bus
L	H	X	X	X	9B data to 9A bus
L	X	L	X	X	10A data to 10B bus
L	X	H	X	X	10B data to 10A bus
L	X	X	L	L	11A data to 11B bus
L	X	X	L	H	11A, 11B isolation
L	X	X	H	X	11B data to 11A bus

[†] OC = Open-collector outputs

logic diagram (positive logic)



SN54ABTE16246, SN74ABTE16246

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABTE16246			SN74ABTE16246			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	\overline{OE}	2			2			V
		Except \overline{OE}	1.6			1.6			
V_{IL}	Low-level input voltage	\overline{OE}			0.8			0.8	V
		Except \overline{OE}			1.4			1.4	
V_{OH}	High-level output voltage	1A–8A			5.5	0		5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	B bus			–12			–12	mA
		9A–11A			–24			–64	
I_{OL}	Low-level output current	B bus			12			12	mA
		A bus			64			90	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: Unused pins (input or A-bus I/O) must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ABTE16246			SN74ABTE16246			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2			V
V _{OH}	B port	V _{CC} = 5.5 V, I _{OH} = −100 μA		V _{CC} −0.2			V _{CC} −0.2			V
		V _{CC} = 4.5 V	I _{OH} = −1 mA	2.4		2.4				
			I _{OH} = −12 mA	2		2				
	9A–11A	V _{CC} = 5.5 V, I _{OH} = −1 mA		4.5			4.5			
		V _{CC} = 4.5 V	I _{OH} = −32 mA	2.4		2.4				
			I _{OH} = −64 mA			2				
I _{OH}	1A–8A	V _{CC} = 4.5 V, V _{OH} = 5.5 V		20			20			μA
V _{OL}	B port	V _{CC} = 4.5 V	I _{OL} = 1 mA	0.4			0.4			V
			I _{OL} = 12 mA				0.8			
	A port	V _{CC} = 4.5 V	I _{OL} = 64 mA	0.55			0.55			
			I _{OL} = 90 mA				0.9			
V _{hys}				100			100			mV
I _I (hold)	B port	V _{CC} = 4.5 V	V _I = 0.8 V	100			100			μA
			V _I = 2 V	−100			−100			
		V _{CC} = 5.5 V, V _I = 0 to 5.5 V	±500			±500				
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND	±1			±1			μA	
	A or B ports		±20			±20				
I _{OZH} [‡]	9A–11A	V _{CC} = 5.5 V, V _O = 2.7 V		10			10			μA
I _{OZL} [‡]	9A–11A	V _{CC} = 5.5 V, V _O = 0.5 V		−10			−10			μA
I _O	A port	V _{CC} = 5.5 V, V _O = 2.5 V		−50	−120	−180	−50		−180	mA
	B port			−25	−52	−90	−25		−90	
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V, V _{CC} BIAS = 0		±100			±100			μA
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	28 36		28 36				mA
			Outputs low	38 48		38 48				
			Outputs disabled	20 32		20 32				
I _{CCD}	A or B ports	V _{CC} = 5 V, C _L = 50 pF	$\overline{\text{OE}}$ high	0.02		0.02				mA/ MHz
			$\overline{\text{OE}}$ low	0.33		0.33				
C _i	Control inputs	V _I = 2.5 V or 0.5 V			2.5	4	2.5	4	pF	
C _{io}	I/O ports	V _O = 2.5 V or 0.5 V			4.5	8	4.5	8	pF	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

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11-BIT INCIDENT-WAVE SWITCHING BUS TRANSCEIVERS

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live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54ABTE16246			SN74ABTE16246			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I _{CC} (V _{CC} BIAS)		V _{CC} = 0 to 4.5 V, V _{CC} BIAS = 4.5 V to 5.5 V, I _O (DC) = 0		250 700			250 700			μA
		V _{CC} = 4.5 V to 5.5 V†, V _{CC} BIAS = 4.5 V to 5.5 V, I _O (DC) = 0		20			20			
V _O	A port	V _{CC} = 0	V _{CC} BIAS = 4.5 V to 5.5 V	1.1	1.5	1.9	1.1	1.5	1.9	V
			V _{CC} BIAS = 4.75 V to 5.25 V	1.3	1.5	1.7	1.3	1.5	1.7	
I _O	A port	V _{CC} = 0	V _O = 0, V _{CC} BIAS = 4.5 V	–20		–100	–20		–100	μA
			V _O = 3 V, V _{CC} BIAS = 4.5 V	20		100	20		100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ V_{CC} – 0.5 V < V_{CC}BIAS

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V T _A = 25°C			SN54ABTE16246		SN74ABTE16246		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	B	1.5	3.1	4.2	1.5	5.4	1.5	5.2	ns
t _{PHL}			1.5	3.5	4.6	1.5	5.4	1.5	5.2	
t _{PLH}	9B–11B	9A–11A	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t _{PHL}			1.5	3.2	4	1.5	4.7	1.5	4.5	
t _{PLH} §	1B–8B	1A–8A	1.5	3.2	4	1.5	4.7	1.5	4.5	ns
t _{PLH} ¶			7.5	8.9	9.7	7.5	10.6	7.5	10.3	
t _{PHL}			1.5	3.2	4	1.5	4.7	1.5	4.5	
t _{PZH}	\overline{OE}	9A–11A	2	4.3	5.3	2	6.4	2	6.2	ns
t _{PZL}		1A–11A	2	4.4	5.4	2	7	2	6.8	
t _{PZH}	\overline{OE}	B	2	4.3	6	2	7.3	2	7.1	ns
t _{PZL}			2	4.5	6.4	2	7.5	2	7.3	
t _{PHZ}	\overline{OE}	9A–11A	2	4.2	5.9	2	7	2	6.7	ns
t _{PLZ}		1A–11A	2	3.5	4.6	2	5.4	2	5.1	
t _{PHZ}	\overline{OE}	B	2.5	4.3	6.2	2.5	7.2	2.5	7	ns
t _{PLZ}			2	3.6	5	2	5.8	2	5.5	

§ Measurement point is V_{OL} + 0.3 V.

¶ Measurement point is V_{OL} + 1.5 V.

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11-BIT INCIDENT-WAVE SWITCHING BUS TRANSCEIVERS
WITH 3-STATE AND OPEN-COLLECTOR OUTPUTS

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extended switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	$V_{CC} = 5$ V $T_A = 25^\circ\text{C}$			SN54ABTE16246		SN74ABTE16246		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	9B–11B	9A–11A	$R_X = 13\ \Omega$	1.5	3.2	4	1.5	5	1.5	4.8	ns
t_{PHL}				1.5	3.8	4.7	1.5	5.8	1.5	5.6	
t_{PHL}	1B–8B	1A–8A	$R_X = 13\ \Omega$	1.5	3.3	4.2	1.5	5	1.5	4.8	ns
t_{PLH}	9B–11B	9A–11A	$R_X = 26\ \Omega$	1.5	3.1	4	1.5	4.8	1.5	4.6	ns
t_{PHL}				1.5	3.5	4.4	1.5	5.2	1.5	4.9	
t_{PHL}	1B–8B	1A–8A	$R_X = 26\ \Omega$	1.5	3.1	4	1.5	4.6	1.5	4.4	ns
t_{PLH}	9B–11B	1A–8A	$R_X = 56\ \Omega$	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t_{PHL}				1.5	3.3	4.2	1.5	5.1	1.5	4.7	
t_{PHL}	1B–8B	1A–8A	$R_X = 56\ \Omega$	1.5	3	4	1.5	4.6	1.5	4.4	ns
$t_{sk(p)}$	B	A	$R_X = \text{Open}$		0.1	0.6		2		2	ns
	A	B			0.4	0.8		2		2	
	B	A	$R_X = 26\ \Omega$		0.3	0.8		2		2	
$t_{sk(o)}$	B	A	$R_X = \text{Open}$		0.3	0.7		1.3		1.3	ns
	A	B			0.7	1.1		1.3		1.3	
	B	A	$R_X = 26\ \Omega$		0.5	1		1.3		1.3	
t_t^\dagger	B	A	$R_X = 26\ \Omega$	0.5	0.8	1.5	0.5	1.5	0.5	1.5	ns
t_t^\ddagger	A	B	Rise or fall time 10%–90%	3.5	5.5	7.3	3.5	8.1	3.5	7.9	ns

$^\dagger t_t$ is measured between 1 V and 2 V of the output waveform.

$^\ddagger t_t$ is measured between 10% and 90% of the output waveform.

NOTE 4: Limits are specified but not production tested.

extended output characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (see Note 4 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LOAD	SN54ABTE16246		SN74ABTE16246		UNIT
					MIN	MAX	MIN	MAX	
$t_{sk(temp)}$	A	B	$V_{CC} = \text{constant},$ $\Delta T_A = 20^\circ\text{C}$			3		2.5	ns
	B	A		$R_X = 56\ \Omega$		4.5		4	
$t_{sk(load)}$	B	A	$V_{CC} = \text{constant},$ Temperature = constant	$R_X = 13, 26,$ or $56\ \Omega$		4.5		4	ns

NOTE 4: Limits are specified but not production tested.

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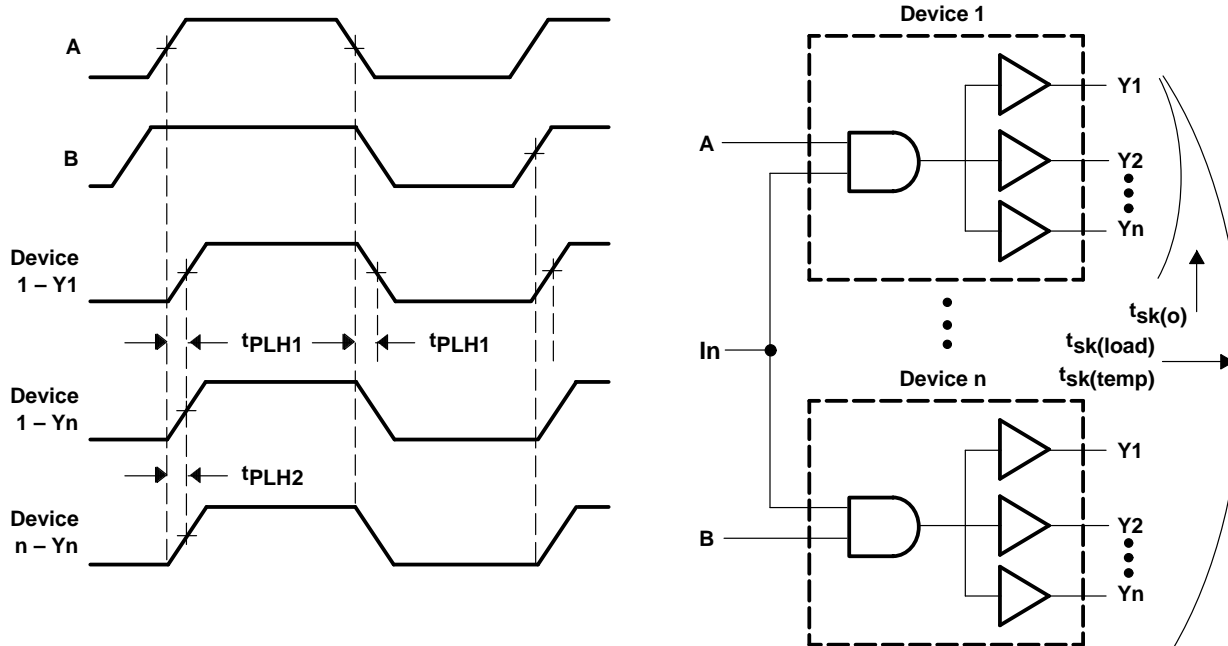
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11-BIT INCIDENT-WAVE SWITCHING BUS TRANSCEIVERS

WITH 3-STATE AND OPEN-COLLECTOR OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. Pulse skew, $t_{sk(p)}$, is defined as the difference in propagation delay times t_{PLH1} and t_{PLH1} on the same terminal at identical operating conditions.
 - B. Output skew, $t_{sk(o)}$, is defined as the difference in propagation delay of the fastest and slowest paths on a single device that originate at either a single input or multiple simultaneously switched inputs (e.g., $|t_{PLH1} - t_{PLH2}|$).
 - C. Temperature skew, $t_{sk(temp)}$, is the output skew of two devices, both having the same value of $V_{CC} \pm 1\%$ and with package temperature differences of 20°C .
 - D. Load skew, $t_{sk(load)}$, is measured with R_X in Figure 2 at $13\ \Omega$ for one unit and $56\ \Omega$ for the other unit.

Figure 1. Voltage Waveforms for Extended Characteristics

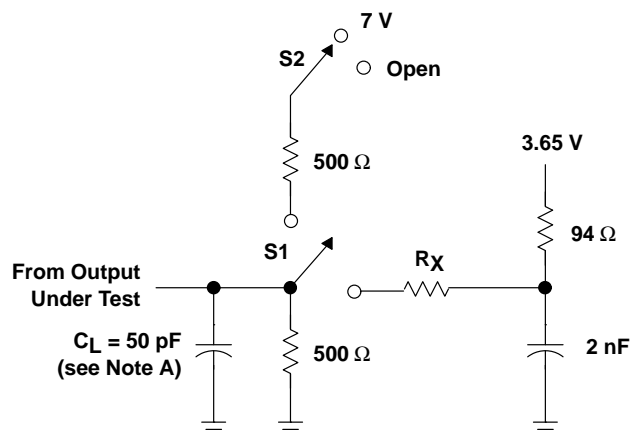
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WITH 3-STATE AND OPEN-COLLECTOR OUTPUTS

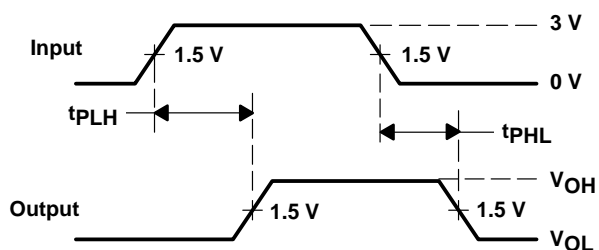
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PARAMETER MEASUREMENT INFORMATION



$R_X = 13\ 26\ \text{or}\ 56\ \Omega$

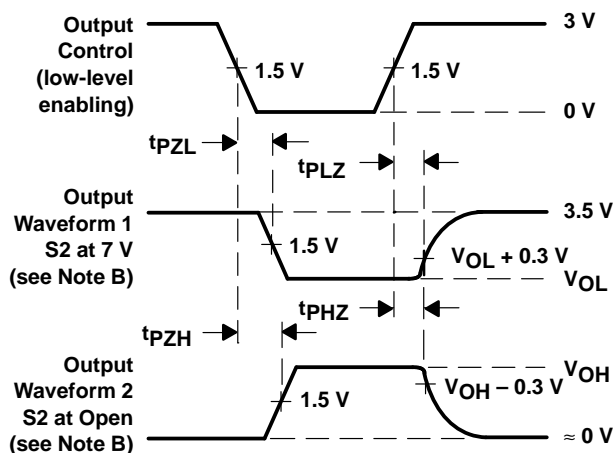
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

SWITCHING TABLE LOADS	S1	S2
t_{PLH}/t_{PHL} (9A–11A and B port)	Up	Open
t_{PLH}/t_{PHL} (1A–8A)	Up	7 V
t_{PLZ}/t_{PZL}	Up	7 V
t_{PHZ}/t_{PZH} (except 1A–8A)	Up	Open

EXTENDED SWITCHING TABLE LOADS	S1	S2
$t_{PLH}/t_{PHL}/t_{sk}$ (A port)	Down	X
$t_{PLH}/t_{PHL}/t_{sk}$ (B port)	Up	Open
t_t (A port) (see Note E)	Down	X
t_t (B port) (see Note F)	Up	Open



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\ \text{MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\ \text{ns}$, $t_f \leq 2.5\ \text{ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_t is measured between 1 V and 2 V of the output waveform.
 - F. t_t is measured between 10% and 90% of the output waveform.

Figure 2. Load Circuit and Voltage Waveforms

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