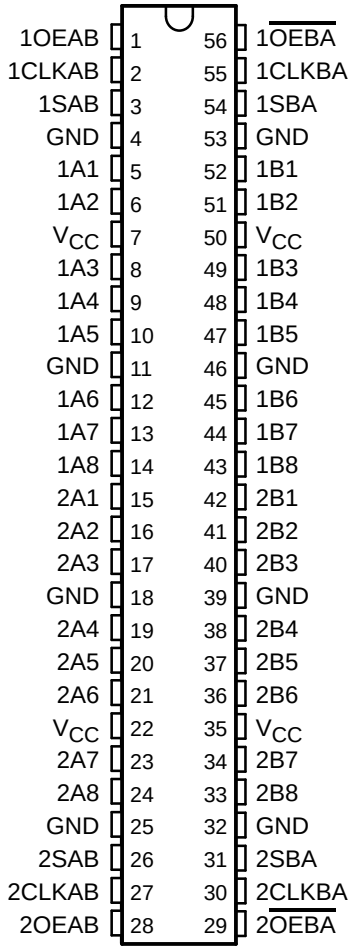
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$)**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54ABT16652 . . . WD PACKAGE**
**SN74ABT16652 . . . DL PACKAGE**
**(TOP VIEW)**




## description

The ’ABT16652 are 16-bit bus transceivers that consist of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. These devices can be used as two 8-bit transceivers or one 16-bit transceiver.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ’ABT16652.

Data on the A- or B-data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control inputs. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

## description (continued)

To ensure the high-impedance state during power up or power down, $\overline{OEBA}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

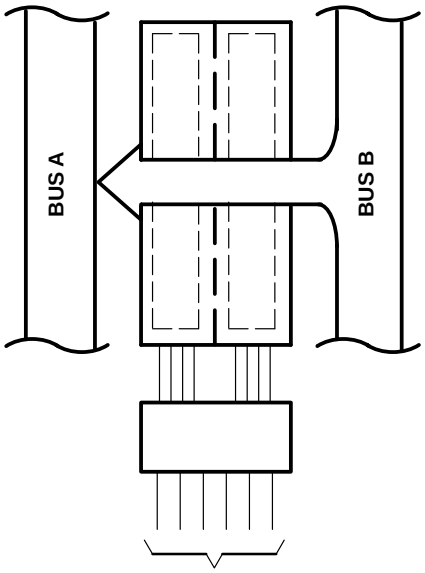
The SN54ABT16652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16652 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | | | | DATA I/O† | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| L | H | H or L | H or L | X | X | Input | Input | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| X | H | ↑ | H or L | X | X | Input | Unspecified‡ | Store A, hold B |
| H | H | ↑ | ↑ | X‡ | X | Input | Output | Store A in both registers |
| L | X | H or L | ↑ | X | X | Unspecified‡ | Input | Hold A, store B |
| L | L | ↑ | ↑ | X | X‡ | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| H | H | H or L | X | H | X | Input | Output | Stored A data to B bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored A data to B bus and stored B data to A bus |

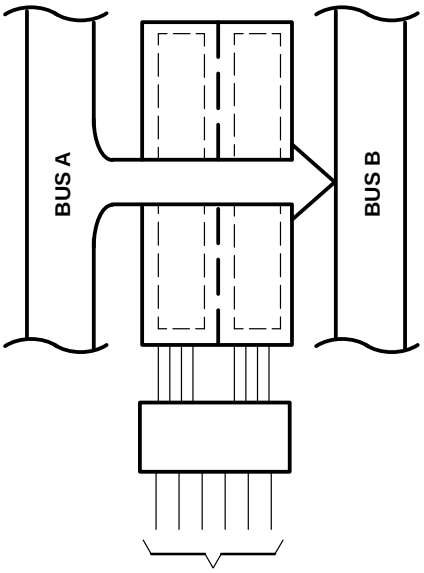
† The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or $\overline{OEBA}$. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered to load both registers.



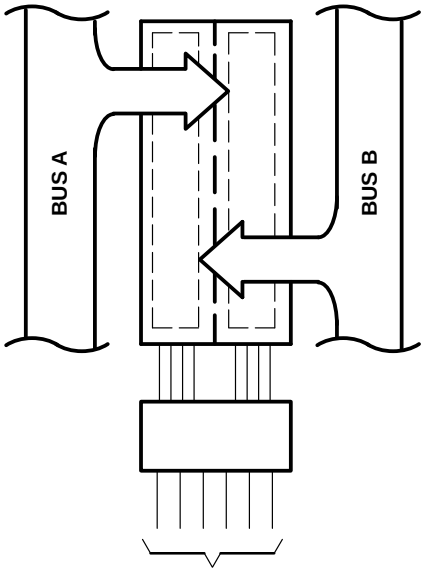

| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**



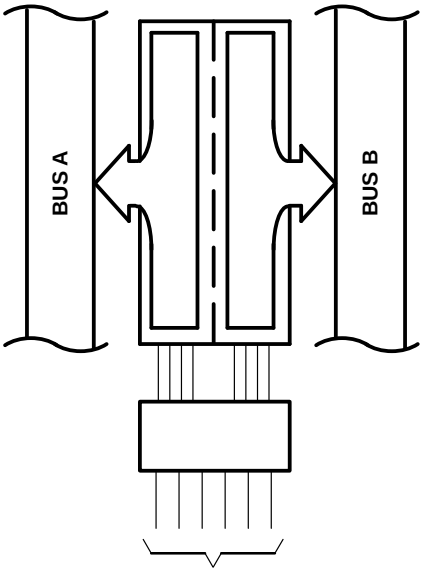

| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| H | H | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**




| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| X | H | ↑ | X | X | X |
| L | X | X | ↑ | X | X |
| L | H | ↑ | ↑ | X | X |

**STORAGE FROM**
**A, B, OR A AND B**

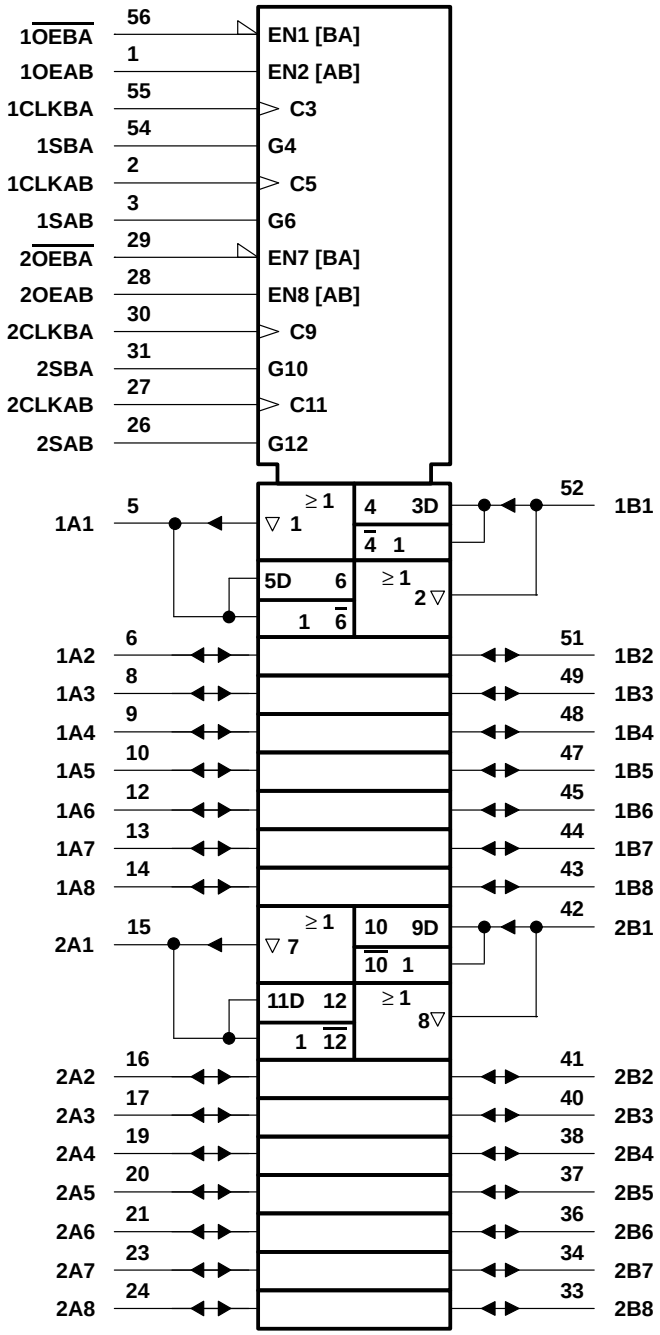



| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| H | L | H or L | H or L | H | H |

**TRANSFER STORED DATA**
**TO A AND/OR B**

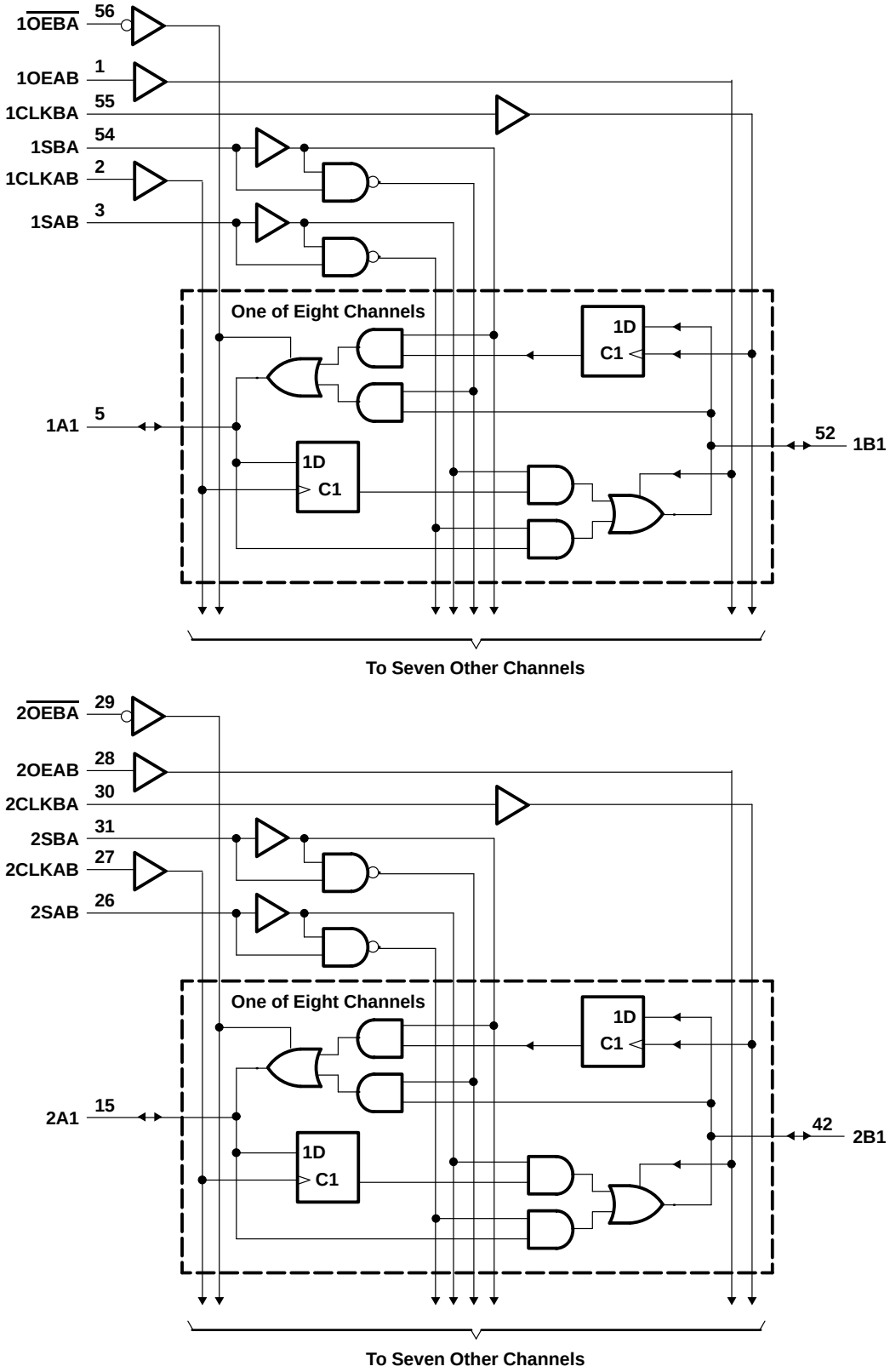
**Figure 1. Bus-Management Functions**

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ . . . . . –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT16652 . . . . . 96 mA
SN74ABT16652 . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –18 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DL package . . . . . 74°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

### recommended operating conditions (see Note 3)

| | | | SN54ABT16652 | | SN74ABT16652 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABT16652 | | SN74ABT16652 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| $V_{hys}$ | | | | | 100 | | | | | | mV |
| $I_I$ | Control inputs | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | | | | | ±20 | | ±20 | | ±20 | |
| $I_{OZH}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 10 | | 10 | | 10 | µA |
| $I_{OZL}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –10 | | –10 | | –10 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O \le$ 4.5 V | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | | $V_{CC}$ = 5.5 V, $V_O$ = 5.5 V | Outputs high | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –100 | –180 | –50 | –180 | –50 | –180 | mA |
| $I_{CC}$ | A or B ports | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | | 2 | | 2 | | 2 | mA |
| | | | Outputs low | | | 32 | | 32 | | 32 | |
| | | | Outputs disabled | | | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | Data inputs | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | Outputs enabled | | | 50 | | 50 | | 50 | µA |
| | | | Outputs disabled | | | 50 | | 50 | | 50 | |
| | Control inputs | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 50 | | 50 | | 50 | |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 4 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 8 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)**

| | | SN54ABT16652 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | MIN | MAX | |
| | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | 0 | 125 | 0 | 125 | MHz |
| $t_w$ | Pulse duration, CLK high or low | 4.3 | | 4.3 | | ns |
| $t_{su}$ | Setup time, A or B before CLKAB↑ or CLKBA↑ | 3.5 | | 4 | | ns |
| $t_h$ | Hold time, A or B after CLKAB↑ or CLKBA↑ | 0.5 | | 0.5 | | ns |

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)**

| | | SN74ABT16652 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | MIN | MAX | |
| | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | 0 | 125 | 0 | 125 | MHz |
| $t_w$ | Pulse duration, CLK high or low | 4.3 | | 4.3 | | ns |
| $t_{su}$ | Setup time, A or B before CLKAB↑ or CLKBA↑ | 3 | | 3 | | ns |
| $t_h$ | Hold time, A or B after CLKAB↑ or CLKBA↑ | 0 | | 0 | | ns |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 2)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT16652 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | 125 | | | 125 | | MHz |
| $t_{PLH}$ | CLK | B or A | 1.5 | 3.1 | 4 | 1 | 5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.2 | 4.1 | 1 | 5 | |
| $t_{PLH}$ | A or B | B or A | 1 | 2.3 | 3.2 | 0.6 | 4 | ns |
| $t_{PHL}$ | | | 1 | 3 | 4.1 | 0.6 | 4.9 | |
| $t_{PLH}$ | SAB or SBA† | B or A | 1 | 2.9 | 4.3 | 0.6 | 5.3 | ns |
| $t_{PHL}$ | | | 1 | 3.1 | 4.6 | 0.6 | 5.3 | |
| $t_{PZH}$ | $\overline{OEBA}$ | A | 1 | 2.8 | 4.1 | 0.6 | 5.2 | ns |
| $t_{PZL}$ | | | 1.5 | 3.1 | 4.4 | 1 | 5.4 | |
| $t_{PHZ}$ | $\overline{OEBA}$ | A | 1.5 | 3.4 | 4.7 | 0.8 | 5.3 | ns |
| $t_{PLZ}$ | | | 1.5 | 2.7 | 4 | 1 | 5.3 | |
| $t_{PZH}$ | OEAB | B | 1 | 2.6 | 3.6 | 0.8 | 4.7 | ns |
| $t_{PZL}$ | | | 1.5 | 2.8 | 4.5 | 1 | 5 | |
| $t_{PHZ}$ | OEAB | B | 2 | 4.2 | 5.9 | 1 | 6.4 | ns |
| $t_{PLZ}$ | | | 1.5 | 3.4 | 4.9 | 1 | 5.9 | |

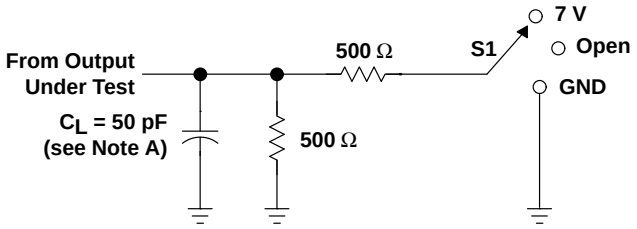
† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 2)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT16652 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | 125 | | | 125 | | MHz |
| $t_{PLH}$ | CLK | B or A | 1.5 | 3.1 | 4 | 1.5 | 4.9 | ns |
| $t_{PHL}$ | | | 1.5 | 3.2 | 4.1 | 1.5 | 4.7 | |
| $t_{PLH}$ | A or B | B or A | 1 | 2.3 | 3.2 | 1 | 3.9 | ns |
| $t_{PHL}$ | | | 1 | 3 | 4.1 | 1 | 4.6 | |
| $t_{PLH}$ | SAB or SBA† | B or A | 1 | 2.9 | 4.3 | 1 | 5 | ns |
| $t_{PHL}$ | | | 1 | 3.1 | 4.3 | 1 | 5 | |
| $t_{PZH}$ | $\overline{OEBA}$ | A | 1 | 2.8 | 4.1 | 1 | 5 | ns |
| $t_{PZL}$ | | | 1.5 | 3.1 | 4.4 | 1.5 | 5.3 | |
| $t_{PHZ}$ | $\overline{OEBA}$ | A | 1.5 | 3.4 | 4.4 | 1.5 | 4.9 | ns |
| $t_{PLZ}$ | | | 1.5 | 2.7 | 3.6 | 1.5 | 4 | |
| $t_{PZH}$ | OEAB | B | 1 | 2.6 | 3.6 | 1 | 4.2 | ns |
| $t_{PZL}$ | | | 1.5 | 2.8 | 3.9 | 1.5 | 4.6 | |
| $t_{PHZ}$ | OEAB | B | 2 | 4.2 | 5.5 | 2 | 5.9 | ns |
| $t_{PLZ}$ | | | 1.5 | 3.4 | 4.5 | 1.5 | 5.2 | |

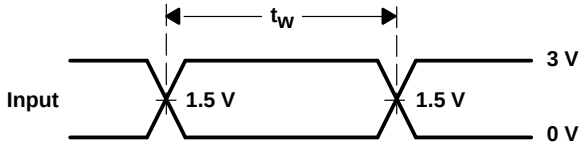
† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

## PARAMETER MEASUREMENT INFORMATION

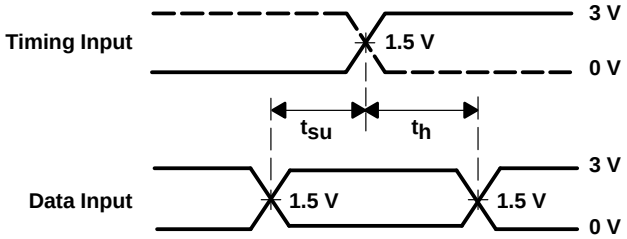



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

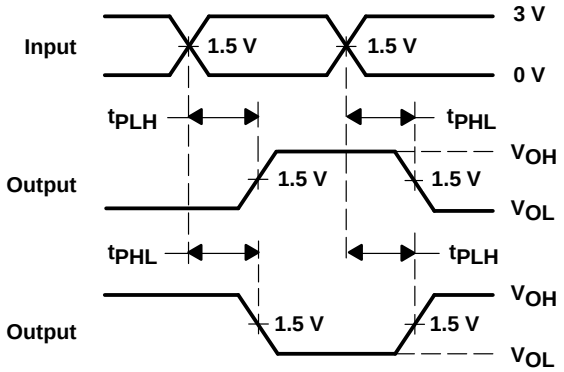
LOAD CIRCUIT



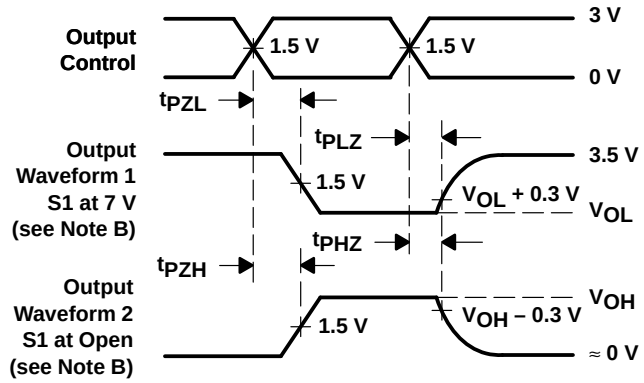

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

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