

SN54ABT16651, SN74ABT16651 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS214 – OCTOBER 1992

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

description

The 'ABT16651 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Output-enable ($OEAB$ and \overline{OEBA}) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16651.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock ($CLKAB$ or $CLKBA$) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling $OEAB$ and \overline{OEBA} . In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

SN54ABT16651 . . . WD PACKAGE
SN74ABT16651 . . . DL PACKAGE
(TOP VIEW)

1OEAB	1	56	1OEBA
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2OEBA

PRODUCT PREVIEW

Widebus and EPIC-II B are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1992, Texas Instruments Incorporated

SN54ABT16651, SN74ABT16651

16-BIT BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS214 – OCTOBER 1992

description (continued)

To ensure the high-impedance state during power up or power down, \overline{OEBA} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

The SN74ABT16651 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16651 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16651 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	\overline{OEBA}	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	\uparrow	\uparrow	X	X	Input	Input	Store A and B data
X	H	\uparrow	H or L	X	X	Input	Unspecified [†]	Store A, hold B
H	H	\uparrow	\uparrow	X [‡]	X	Input	Output	Store A in both registers
L	X	H or L	\uparrow	X	X	Unspecified [†]	Input	Hold A, store B
L	L	\uparrow	\uparrow	X	X [‡]	Output	input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time \overline{B} data to A bus
L	L	X	H or L	X	H	Output	Output	Stored \overline{B} data to A bus
H	H	X	X	L	X	Input	Output	Real-time \overline{A} data to B bus
H	H	H or L	X	H	X	Input	Output	Stored \overline{A} data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored \overline{A} data to B bus and stored B data to A bus

[†] The data output functions may be enabled or disabled by various signals at the OEAB or \overline{OEBA} inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

[‡] When select control is low, clocks can occur simultaneously so long as allowances are made for propagation delays from A to B (B to A) plus setup and hold times. When select control is high, clocks must be staggered in order to load both registers.

PRODUCT PREVIEW



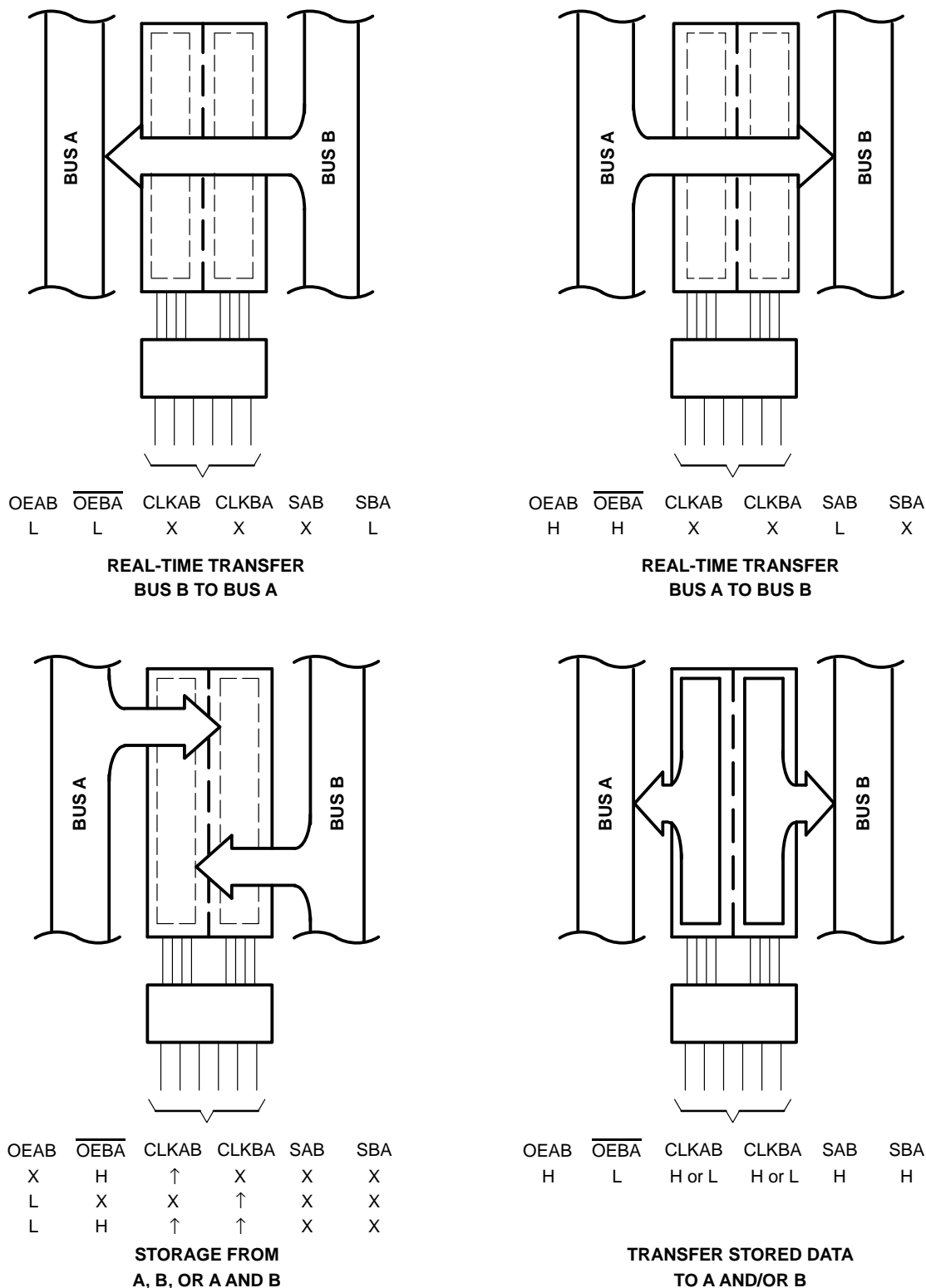


Figure 1. Bus-Management Functions

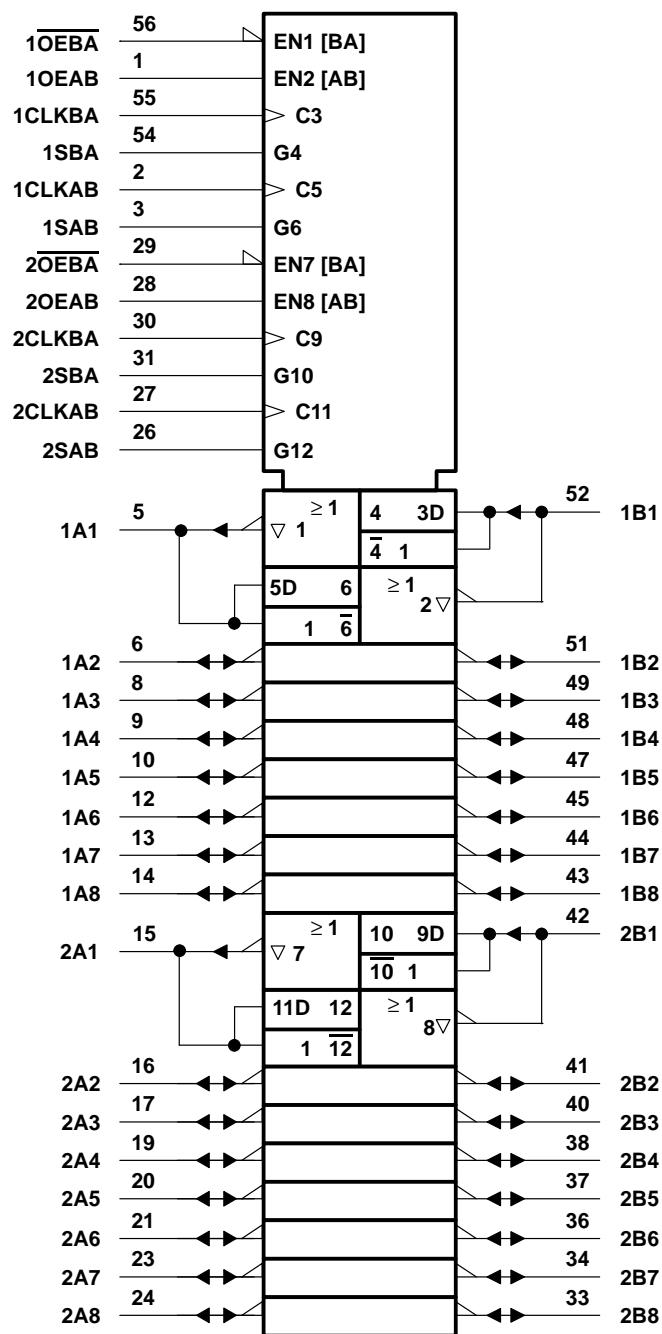
SN54ABT16651, SN74ABT16651

16-BIT BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS214 – OCTOBER 1992

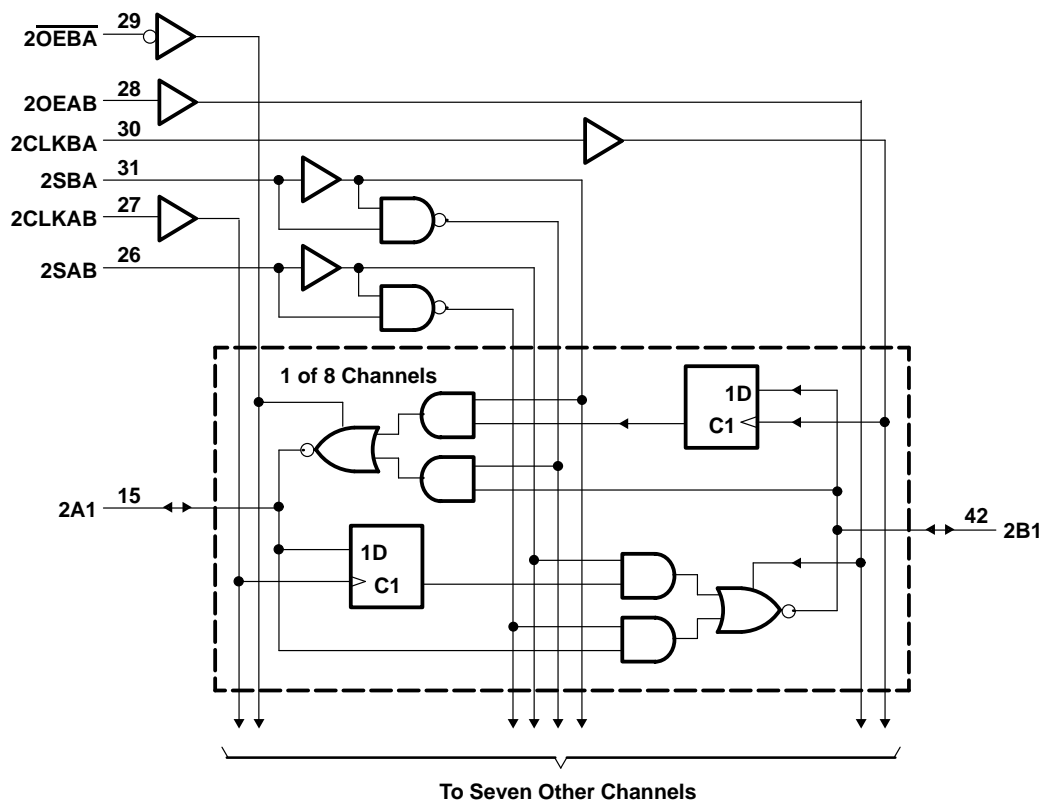
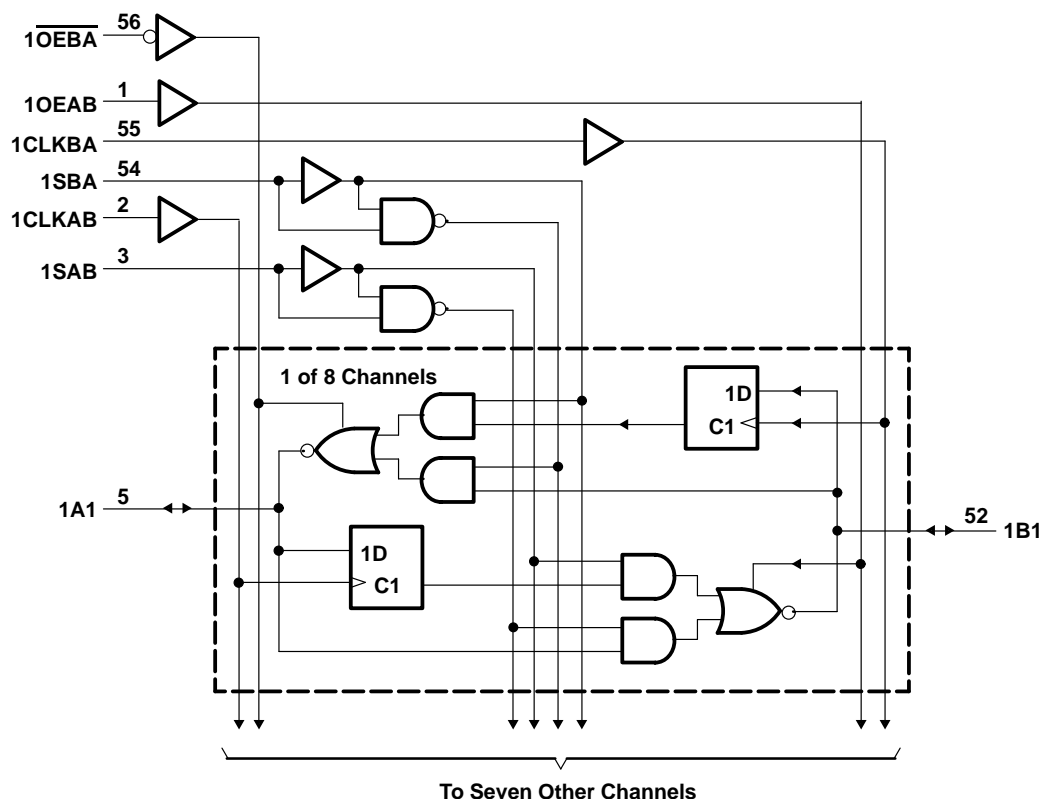
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

SN54ABT16651, SN74ABT16651

16-BIT BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS214 – OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16651	96 mA
SN74ABT16651	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air)	1 W
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT16651		SN74ABT16651		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
	Outputs enabled					
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW



SN54ABT16651, SN74ABT16651
16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

SCBS214 – OCTOBER 1992

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT16651		SN74ABT16651		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA				-1.2		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = -3 mA		3			3		3		
	V _{CC} = 4.5 V, I _{OH} = -24 mA		2			2				
	V _{CC} = 4.5 V, I _{OH} = -32 mA		2‡					2		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA				0.55		0.55			V
	V _{CC} = 4.5 V, I _{OL} = 64 mA				0.55‡				0.55	
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND	Control inputs			±1		±1		±1	μA
		A or B ports			±100		±100		±100	
I _{OZH} §	V _{CC} = 5.5 V, V _O = 2.7 V				50		50		50	μA
I _{OZL} §	V _{CC} = 5.5 V, V _O = 0.5 V				-50		-50		-50	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V				±100				±100	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50		50		50	μA
I _O ¶	V _{CC} = 5.5 V, V _O = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	A or B ports			Outputs high		2		2	mA
					Outputs low		72		72	
					Outputs disabled		2		2	
ΔI _{CC} #	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Data inputs			Outputs enabled		1		1.5	mA
					Outputs disabled		0.05		0.05	
		Control inputs					1.5		1.5	
C _i	V _I = 2.5 V or 0.5 V	Control inputs								pF
C _{io}	V _O = 2.5 V or 0.5 V	A or B ports								pF

† All typical values are at V_{CC} = 5 V.

‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.