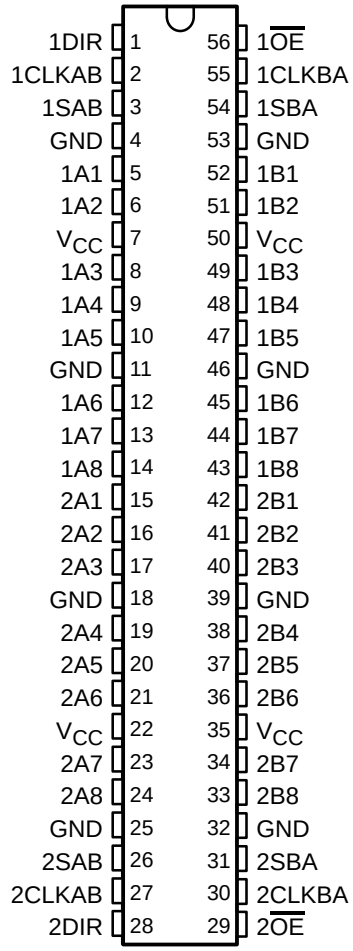
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16648 . . . WD PACKAGE
SN74ABT16648 . . . DL PACKAGE
(TOP VIEW)



description

The ′ABT16648 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ′ABT16648.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus will receive data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16648 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16648 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16648 is characterized for operation from –40°C to 85°C.

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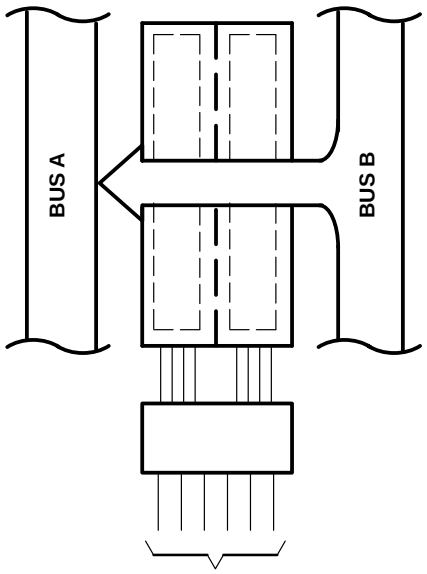
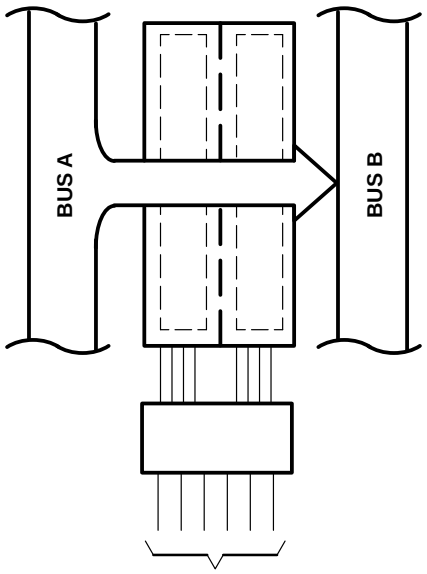


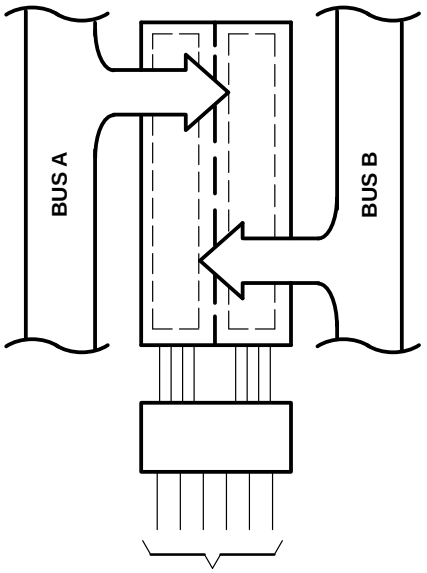
56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



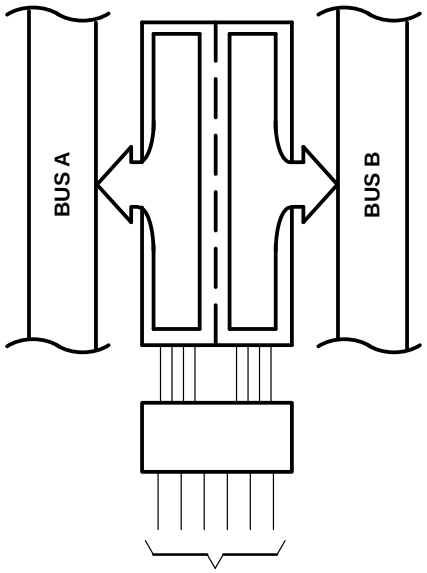
56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

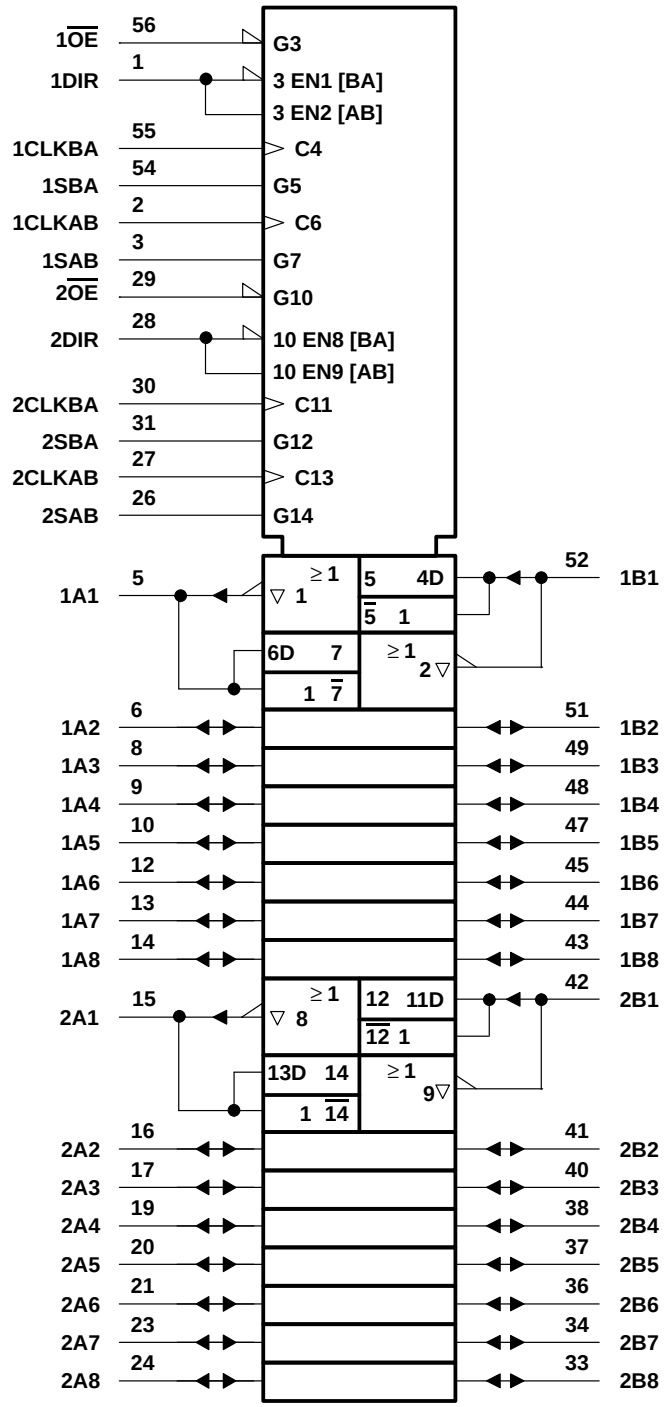


56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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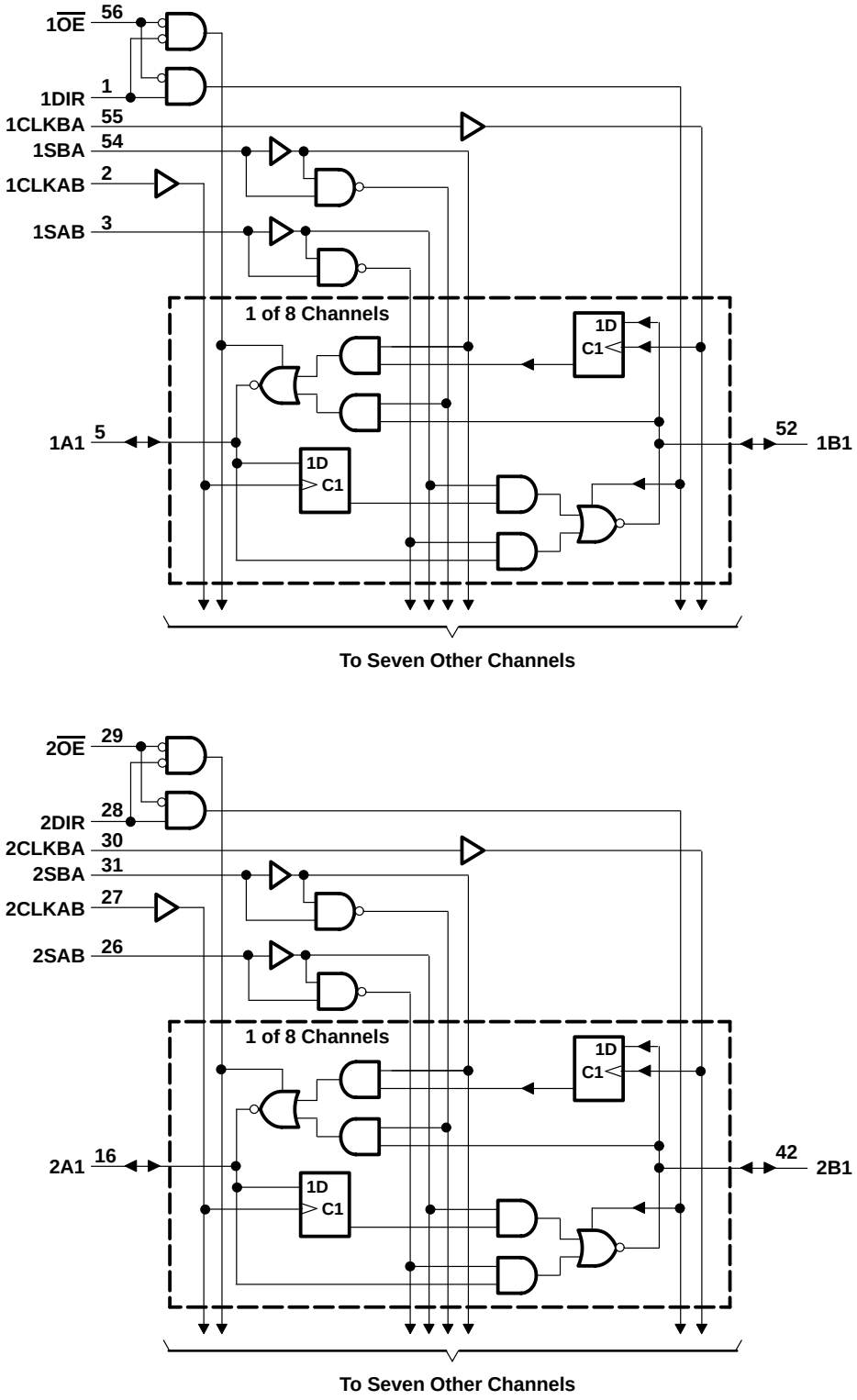
logic diagram (positive logic)



FUNCTION TABLE
(each 8-bit section)

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
L	H	L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus

† The data output functions may be enabled or disabled by a variety of level combinations at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16648 . . . . . 96 mA
SN74ABT16648 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) . . . . . 1 W
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16648		SN74ABT16648		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16648		SN74ABT16648		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = – 24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					–50		–50		–50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			72		72		30	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs								pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports								pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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