

# SN54ABT16623, SN74ABT16623 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS211B – FEBRUARY 1991 – REVISED JANUARY 1997

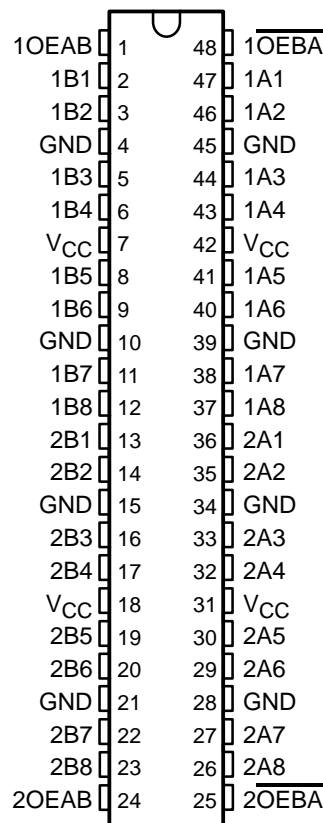
- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

## description

The 'ABT16623 are 16-bit transceivers designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing. The 'ABT16623 provide true data at the outputs.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable (OEAB and  $\overline{\text{OEBA}}$ ) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and  $\overline{\text{OEBA}}$ . Each output reinforces its input in this configuration. When both OEAB and  $\overline{\text{OEBA}}$  are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (32 total) remain at their last states.

SN54ABT16623 . . . WD PACKAGE  
SN74ABT16623 . . . DGG OR DL PACKAGE  
(TOP VIEW)



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**TEXAS  
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SN54ABT16623, SN74ABT16623

16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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description (continued)

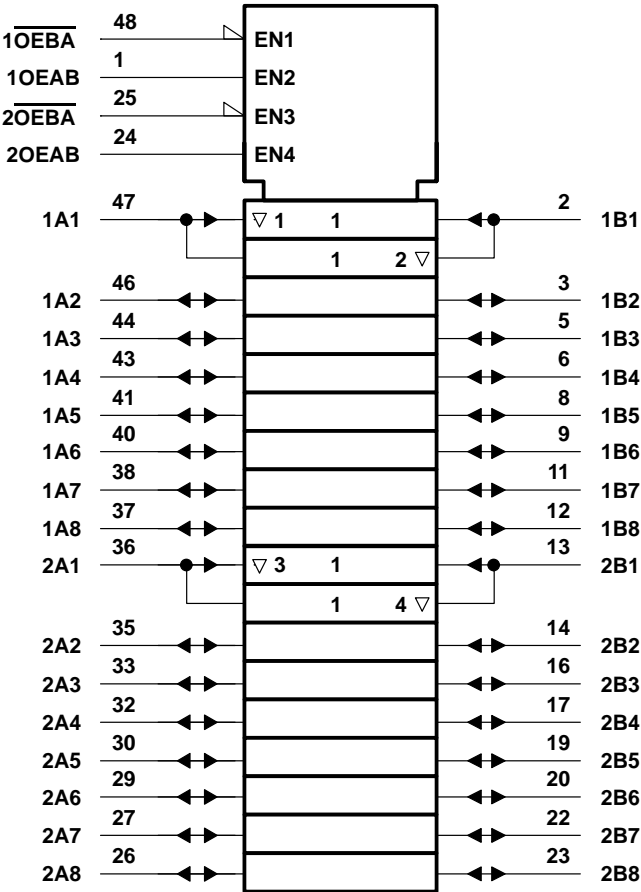
To ensure the high-impedance state during power up or power down,  $\overline{OEBA}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT16623 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ABT16623 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each 8-bit section)

INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	B data to A bus
L	H	B data to A bus, A data to B bus
H	L	Isolation
H	H	A data to B bus

logic symbol†

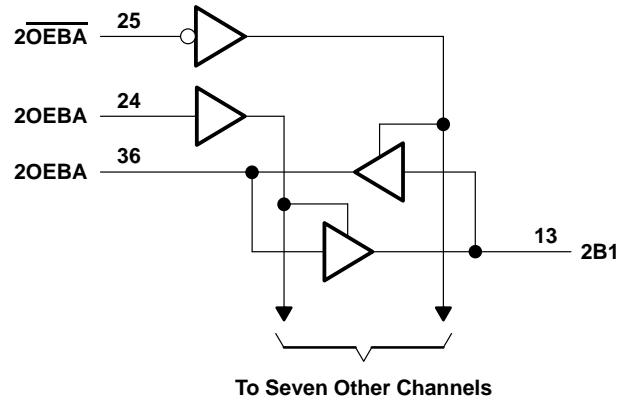
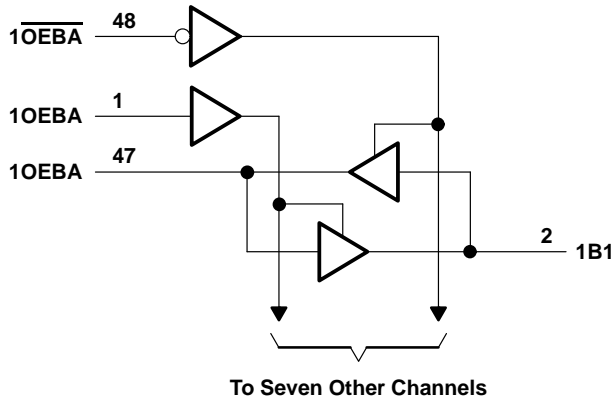


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16623	96 mA
SN74ABT16623	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions (see Note 3)

		SN54ABT16623		SN74ABT16623		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			5	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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## 16-BIT BUS TRANSCEIVERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16623		SN74ABT16623		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5			2.5		2.5		V
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3			3		3		
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA	2			2				
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA	2*					2		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA			0.55		0.55			V
		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA			0.55*				0.55	
V <sub>hys</sub>				100						mV
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μA
	A or B ports				±100		±100		±100	
I <sub>OZH</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			50		50		50	μA
I <sub>OZL</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			-50		-50		-50	μA
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μA
I <sub>CEX</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V, Outputs high			50		50		50	μA
I <sub>O</sub> §		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, Outputs high			2		2		2	mA
		I <sub>O</sub> = 0, Outputs low			35		35		35	
		V <sub>I</sub> = V <sub>CC</sub> or GND, Outputs disabled			2		2		2	
ΔI <sub>CC</sub> ¶	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			1		1.5		1	mA
					0.05		0.05		0.05	
	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			1.5		1.5		1.5	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V			3					pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V			8					pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT16623		SN74ABT16623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	1	2	3.2	1	3.7	1	3.6	ns
$t_{PHL}$			1	2.2	3.4	1	4.4	1	4.3	
$t_{PZH}$	$\overline{\text{OEBA}}$ or OEAB	A or B	1.1	3	4	1.1	5	1.1	4.9	ns
$t_{PZL}$			1.4	3.3	4.9	1.4	6.2	1.4	6	
$t_{PHZ}$	$\overline{\text{OEBA}}$ or OEAB	A or B	1	3.5	4.9	1	6.2	1	6	ns
$t_{PLZ}$			1.4	2.8	4.7	1.4	5.6	1.4	5.4	

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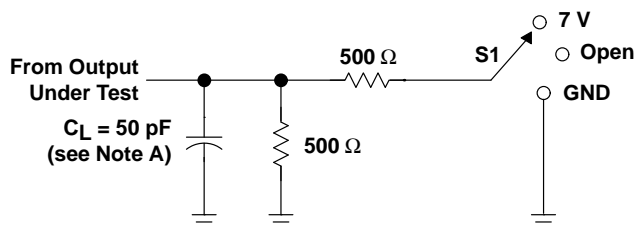
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## 16-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

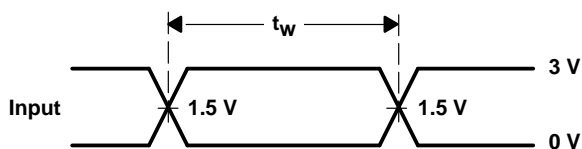
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#### PARAMETER MEASUREMENT INFORMATION

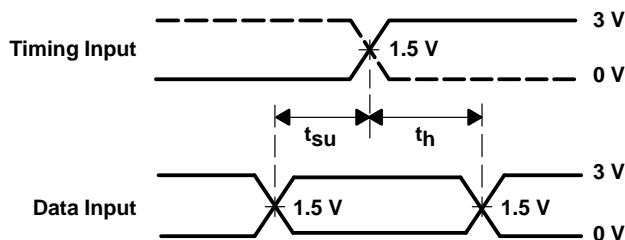


LOAD CIRCUIT

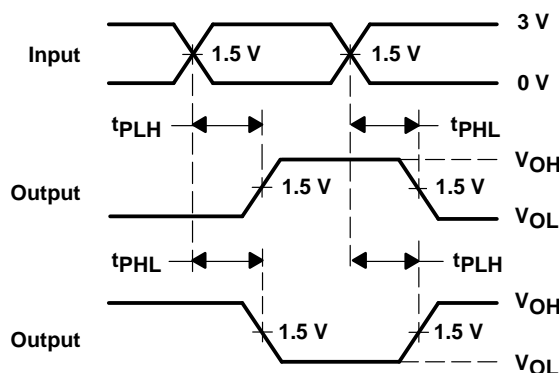
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



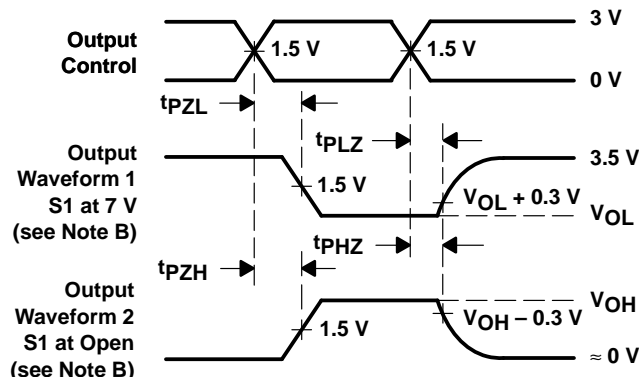
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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