

SN54ABT16601, SN74ABT16601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS210C – JUNE 1992 – REVISED JANUARY 1997

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-II B™ BiCMOS Design Significantly Reduces Power Dissipation**
- **UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, clocked, and clock-enabled modes.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (\overline{LEAB} and \overline{LEBA}), and clock (\overline{CLKAB} and \overline{CLKBA}) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when \overline{LEAB} is high. When \overline{LEAB} is low, the A data is latched if \overline{CLKAB} is held at a high or low logic level. If \overline{LEAB} is low, the A data is stored in the latch/flip-flop on the low-to-high transition of \overline{CLKAB} . Output enable \overline{OEAB} is active low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses \overline{OEBA} , \overline{LEBA} , \overline{CLKBA} , and $\overline{CLKENBA}$.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16601 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16601 is characterized for operation from -40°C to 85°C .

SN54ABT16601 . . . WD PACKAGE
SN74ABT16601 . . . DGG OR DL PACKAGE
(TOP VIEW)

\overline{OEAB}	1	56	$\overline{CLKENAB}$
\overline{LEAB}	2	55	\overline{CLKAB}
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V_{CC}	7	50	V_{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V_{CC}	22	35	V_{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
\overline{OEBA}	27	30	\overline{CLKBA}
\overline{LEBA}	28	29	$\overline{CLKENBA}$



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**TEXAS
INSTRUMENTS**

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SN54ABT16601, SN74ABT16601

18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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FUNCTION TABLE†

INPUTS					OUTPUT B
CLKENAB	OEAB	LEAB	CLKAB	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ ‡
H	L	L	X	X	B ₀ ‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B ₀ ‡
L	L	L	H	X	B ₀ §

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

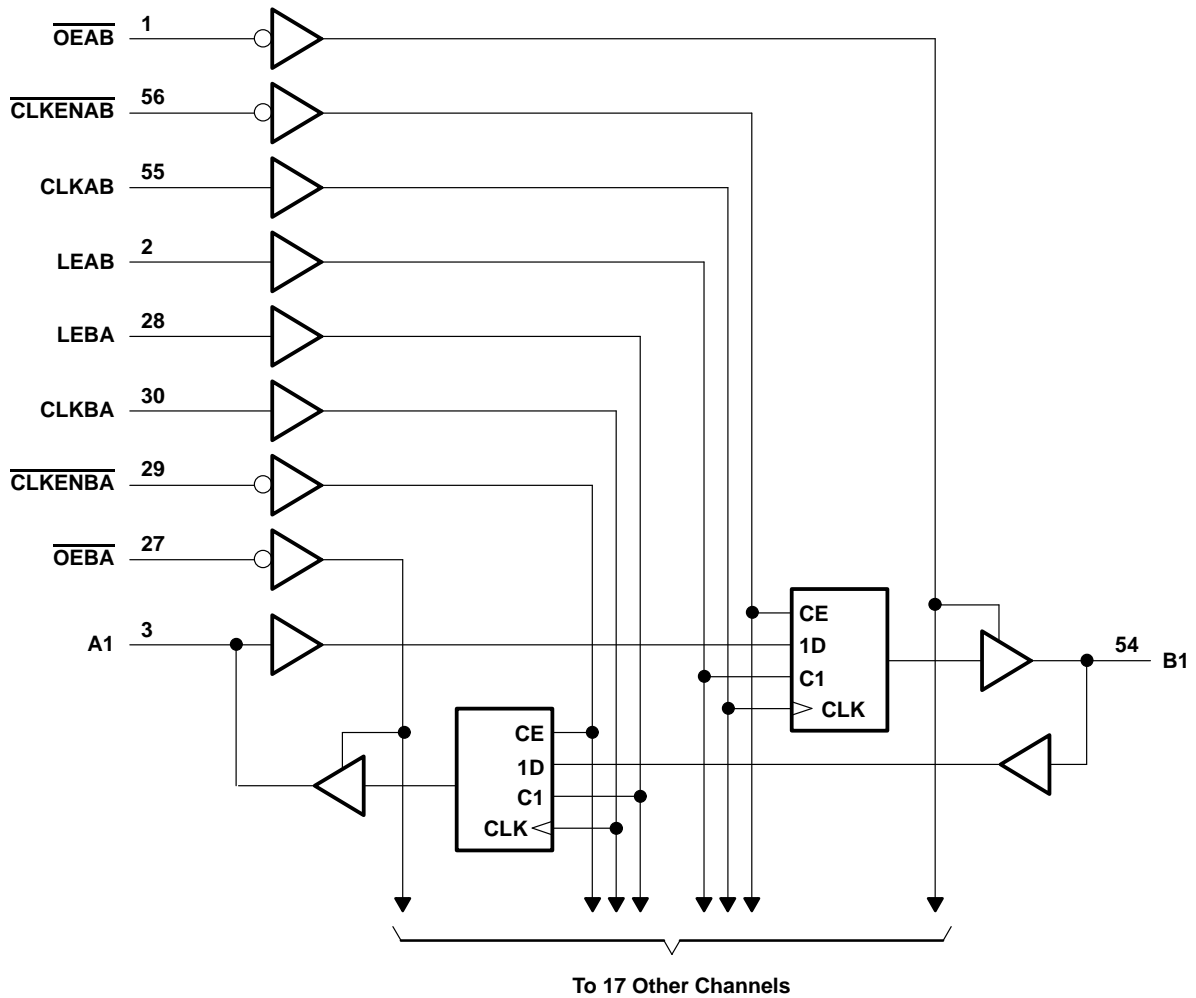
‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_{OL} : SN54ABT16601	96 mA
SN74ABT16601	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.



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recommended operating conditions (see Note 3)

			SN54ABT16601		SN74ABT16601		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT16601		SN74ABT16601		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			–1.2		–1.2		–1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			2.5		2.5		V
		$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			3		3		
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -24\text{ mA}$	2			2				
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -32\text{ mA}$	2*					2		
V_{OL}		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$			0.55		0.55			V
		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 64\text{ mA}$			0.55*				0.55	
V_{hys}				100						mV
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND		± 1		± 1		± 1		μA
	A or B ports			$\pm 20^{**}$		± 100		± 20		
I_{off}		$V_{CC} = 0$, V_I or $V_O \leq 4.5\text{ V}$		± 100				± 100		μA
I_{CEX}		$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$, Outputs high		50		50		50		μA
I_O^\ddagger		$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	–50	–100	–180	–50	–180	–50	–180	mA
I_{OZH}^\S		$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$		10		10		10		μA
I_{OZL}^\S		$V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$		–10		–10		–10		μA
I_{CC}	A or B ports	$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND, Outputs high		1.9	3		2		3	mA
		Outputs low		28	36		35		36	
		Outputs disabled		1.6	3		2		3	
ΔI_{CC}^\P		$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND		50				50		μA
						1.5				mA
C_i	Control inputs	$V_I = 2.5\text{ V}$ or 0.5 V		3						pF
C_{io}	A or B ports	$V_O = 2.5\text{ V}$ or 0.5 V		9						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

** This limit applies only to the SN74ABT16601.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT16601		SN74ABT16601		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high	2.5		2.5		ns
		CLKAB or CLKBA high or low	3		3		
t_{su}	Setup time	A before CLKAB \uparrow or B before CLKBA \uparrow	4.6		4		ns
		A before LEAB \downarrow or B before LEBA \downarrow	CLK high	2.5	2.5		
			CLK low	1.3	1		
		CLKEN before CLK \uparrow	2.9		2.5		
t_h	Hold time	A after CLKAB \uparrow or B after CLKBA \uparrow	0.4		0		ns
		A after LEAB \downarrow or B after LEBA \downarrow	2.8		2		
		CLKEN after CLK \uparrow	0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16601				UNIT	
			V _{CC} = 5 V, T _A = 25°C			MIN		MAX
			MIN	TYP	MAX			
f _{max}			150	200		150	MHz	
t _{PLH}	A or B	B or A	1.5	2.5	4.1	1	4.6	ns
t _{PHL}			1.5	3.4	4.7	1	5.1	
t _{PLH}	LEAB or LEBA	B or A	2	3.4	4.7	1	5.6	ns
t _{PHL}			2	3.7	5	1	5.5	
t _{PLH}	CLKAB or CLKBA	B or A	1.5	3.2	4.5	1	5.2	ns
t _{PHL}			1.5	3.2	4.4	1	5	
t _{PZH}	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	B or A	2	4	5	1	5.7	ns
t _{PZL}			2	4.2	5.6	1	6	
t _{PHZ}	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	B or A	2	4.5	5.8	1	6.8	ns
t _{PLZ}			1.5	3.4	5.3	1	6.3	

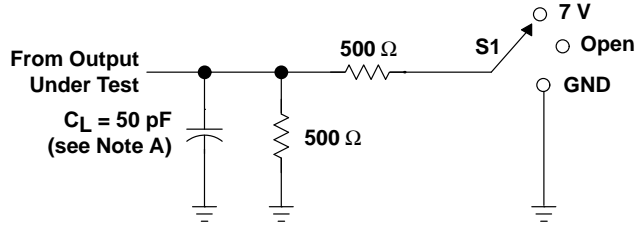
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

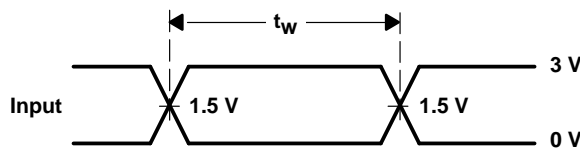
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16601					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f _{max}			150	200		150		MHz
t _{PLH}	A or B	B or A	1.5	2.5	3.6	1.5	4	ns
t _{PHL}			1.5	3.4	4.7	1.5	4.9	
t _{PLH}	LEAB or LEBA	B or A	2	3.4	4.7	2	5	ns
t _{PHL}			2	3.7	5	2	5.2	
t _{PLH}	CLKAB or CLKBA	B or A	1.5	3.2	4.5	1.5	4.7	ns
t _{PHL}			1.5	3.2	4.4	1.5	4.6	
t _{PZH}	\overline{OEAB} or \overline{OEBA}	B or A	2	4	5	2	5.5	ns
t _{PZL}			2	4.2	5.6	2	5.8	
t _{PHZ}	\overline{OEAB} or \overline{OEBA}	B or A	2	4.5	5.4	2	6.2	ns
t _{PLZ}			1.5	3.4	4.7	1.5	5.4	

PARAMETER MEASUREMENT INFORMATION

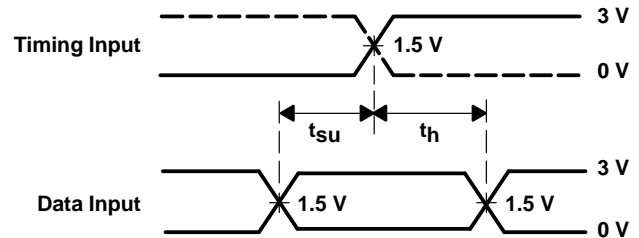


LOAD CIRCUIT

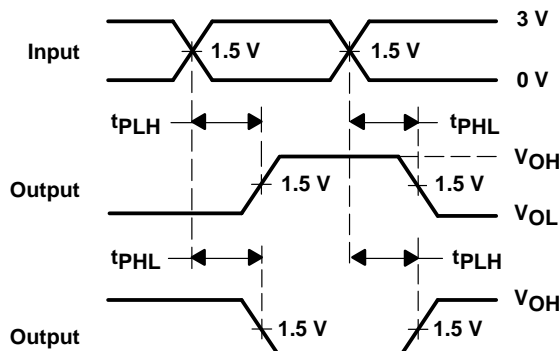
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



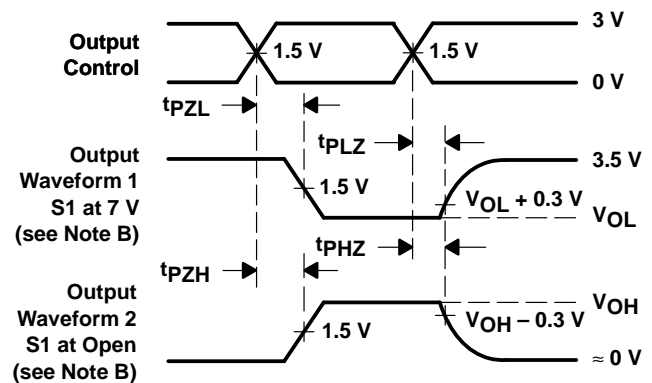
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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