- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**

- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**

- **High-Impedance State During Power Up and Power Down**

- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**

- **High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$)**

- **Package Options Include Plastic Small-Outline (DW) Package, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs**
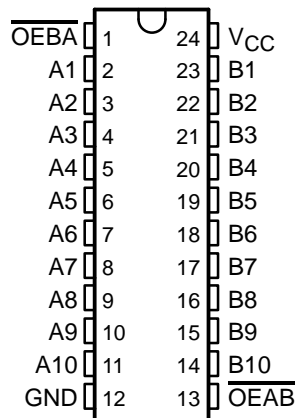
### description

The 'ABT861 are 10-bit transceivers designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.

These devices allow noninverted data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) inputs.
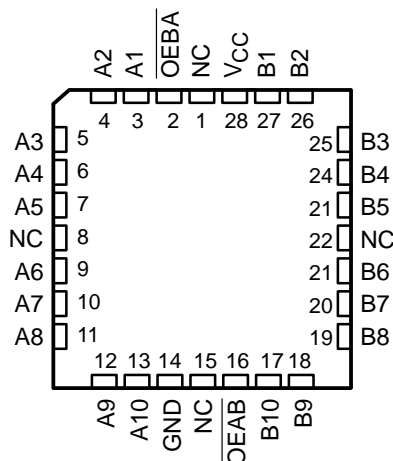
When $V_{CC}$ is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT861 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT861 is characterized for operation from –40°C to 85°C.

**SN54ABT861 . . . JT PACKAGE**
**SN74ABT861 . . . DW OR NT PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| $\overline{OEBA}$ | 1 | 24 | $V_{CC}$ |
| A1 | 2 | 23 | B1 |
| A2 | 3 | 22 | B2 |
| A3 | 4 | 21 | B3 |
| A4 | 5 | 20 | B4 |
| A5 | 6 | 19 | B5 |
| A6 | 7 | 18 | B6 |
| A7 | 8 | 17 | B7 |
| A8 | 9 | 16 | B8 |
| A9 | 10 | 15 | B9 |
| A10 | 11 | 14 | B10 |
| GND | 12 | 13 | $\overline{OEAB}$ |

**SN54ABT861 . . . FK PACKAGE**
**(TOP VIEW)**

Top pins: A2 (4), A1 (3), $\overline{OEBA}$ (2), NC (1), $V_{CC}$ (28), B1 (27), B2 (26)

| | | | |
|---|---|---|---|
| A3 | 5 | 25 | B3 |
| A4 | 6 | 24 | B4 |
| A5 | 7 | 21 | B5 |
| NC | 8 | 22 | NC |
| A6 | 9 | 21 | B6 |
| A7 | 10 | 20 | B7 |
| A8 | 11 | 19 | B8 |

Bottom pins: A9 (12), A10 (13), GND (14), NC (15), $\overline{OEAB}$ (16), B10 (17), B9 (18)

NC – No internal connection

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**FUNCTION TABLE**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OEAB}$ | $\overline{OEBA}$ | |
| L | H | A data to B bus |
| H | L | B data to A bus |
| H | H | Isolation |
| L | L | Latch A and B (A = B) |

## logic symbol[†]
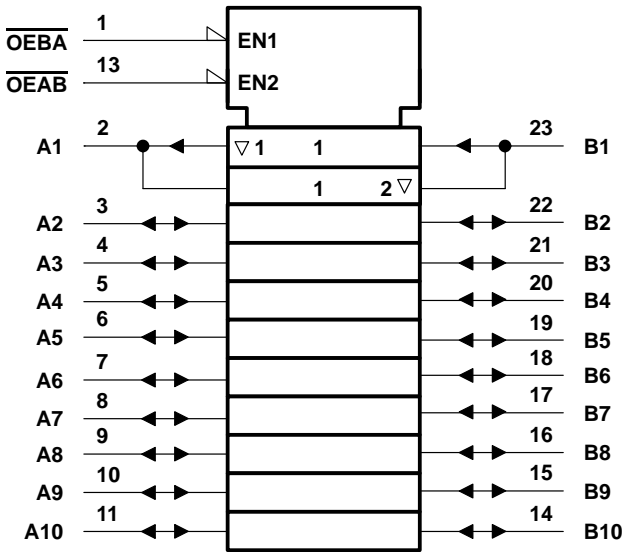


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

## logic diagram (positive logic)
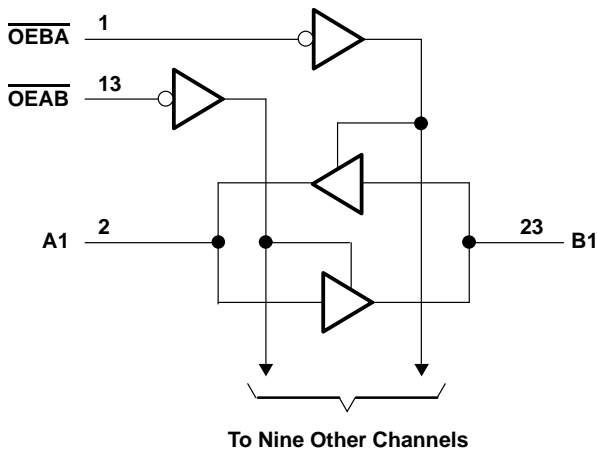


**To Nine Other Channels**

Pin numbers shown are for the DW, JT, and NT packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ............................................................. −0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .................................... −0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .................... −0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT861 .................................... 96 mA
SN74ABT861 .................................... 128 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) ........................................................ −18 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) ...................................................... −50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package ................................ 81°C/W
NT package ................................ 67°C/W
Storage temperature range, $T_{stg}$ ........................................................ −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54ABT861 | | SN74ABT861 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | −24 | | −32 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 5 | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A = 25°C$ | | | SN54ABT861 | | SN74ABT861 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC} = 4.5$ V, | $I_I = -18$ mA | | | −1.2 | | −1.2 | | −1.2 | V |
| $V_{OH}$ | | $V_{CC} = 4.5$ V, | $I_{OH} = -3$ mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC} = 5$ V, | $I_{OH} = -3$ mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC} = 4.5$ V | $I_{OH} = -24$ mA | 2 | | | 2 | | | | |
| | | | $I_{OH} = -32$ mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC} = 4.5$ V | $I_{OL} = 48$ mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL} = 64$ mA | | | 0.55* | | | | 0.55 | |
| $V_{hys}$ | | | | | 100 | | | | | | mV |
| $I_I$ | Control inputs | $V_{CC} = 5.5$ V, | $V_I = V_{CC}$ or GND | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | | | | | ±100 | | ±100 | | ±100 | |
| $I_{OZPU}$‡ | | $V_{CC} = 0$ to 2.1 V, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$ | | | | ±50 | | ±50 | | ±50 | µA |
| $I_{OZPD}$‡ | | $V_{CC} = 2.1$ V to 0, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$ | | | | ±50 | | ±50 | | ±50 | µA |
| $I_{OZH}$§ | | $V_{CC} = 5.5$ V, | $V_O = 2.7$ V | | | 50 | | 50 | | 50 | µA |
| $I_{OZL}$§ | | $V_{CC} = 5.5$ V, | $V_O = 0.5$ V | | | −50 | | −50 | | −50 | µA |
| $I_{off}$ | | $V_{CC} = 0$, | $V_I$ or $V_O \leq 4.5$ V | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | | $V_{CC} = 5.5$ V, $V_O = 5.5$ V | Outputs high | | | 50 | | 50 | | 50 | µA |
| $I_O$¶ | | $V_{CC} = 5.5$ V, | $V_O = 2.5$ V | −50 | −100 | −225# | −50 | −225# | −50 | −225# | mA |
| $I_{CC}$ | A or B ports | $V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND | Outputs high | | 1 | 250 | | 250 | | 250 | µA |
| | | | Outputs low | | 24 | 38 | | 38 | | 38 | mA |
| | | | Outputs disabled | | 0.5 | 250 | | 250 | | 250 | µA |
| $\Delta I_{CC}$‖ | Data inputs | $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | Outputs enabled | | | 1.5 | | 1.5 | | 1.5 | mA |
| | | | Outputs disabled | | | 1.5# | | 1.5# | | 1.5# | |
| | Control inputs | $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | |
| $C_i$ | Control inputs | $V_I = 2.5$ V or 0.5 V | | | 4.5 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O = 2.5$ V or 0.5 V | | | 10.5 | | | | | | pF |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at $V_{CC} = 5$ V.

‡ This parameter is characterized, but not production tested.

§ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# This limit may vary among suppliers.

‖ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

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**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT861 | | SN74ABT861 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1 | 3.4 | 4.9 | 1 | 5.3 | 1 | 5.2 | ns |
| $t_{PHL}$ | | | 1 | 3.2 | 4.4 | 1 | 5 | 1 | 4.9† | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 1 | 3.5 | 5 | 1 | 6 | 1 | 5.9 | ns |
| $t_{PZL}$ | | | 1 | 4.6 | 6 | 1 | 7 | 1 | 6.9 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2.1 | 5.3 | 6.5 | 2.1 | 7.6 | 2.1 | 7.5 | ns |
| $t_{PLZ}$ | | | 1.5 | 5.3 | 6.6 | 1.5 | 7.2 | 1.5 | 7.1 | |

† This limit may vary among suppliers.

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## PARAMETER MEASUREMENT INFORMATION

**From Output Under Test**

500 Ω

**S1**

7 V

Open

GND

$C_L$ = 50 pF (see Note A)

500 Ω
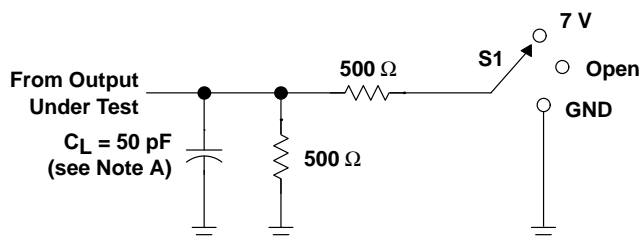
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

**LOAD CIRCUIT**
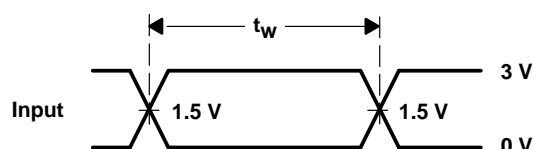
**VOLTAGE WAVEFORMS**
**PULSE DURATION**

Input — $t_w$ — 1.5 V / 1.5 V — 3 V / 0 V
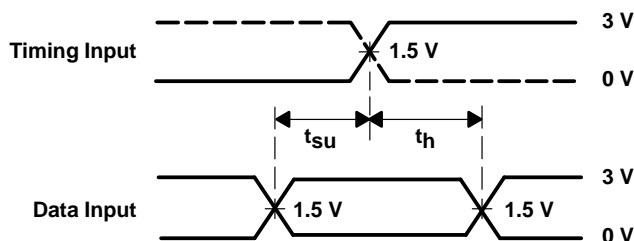
**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**

Timing Input — 1.5 V — 3 V / 0 V

Data Input — $t_{su}$ — $t_h$ — 1.5 V / 1.5 V — 3 V / 0 V
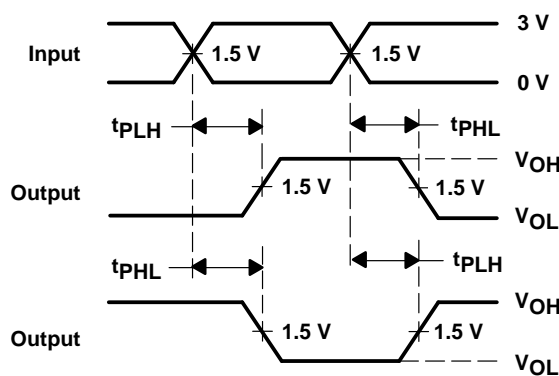
**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**

Input — 1.5 V / 1.5 V — 3 V / 0 V

$t_{PLH}$ — $t_{PHL}$ — Output — 1.5 V / 1.5 V — $V_{OH}$ / $V_{OL}$

$t_{PHL}$ — $t_{PLH}$ — Output — 1.5 V / 1.5 V — $V_{OH}$ / $V_{OL}$
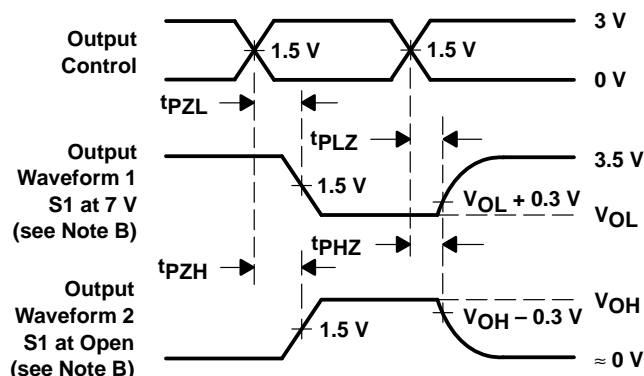
**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**
**LOW- AND HIGH-LEVEL ENABLING**

Output Control — 1.5 V / 1.5 V — 3 V / 0 V

$t_{PZL}$ — $t_{PLZ}$ — Output Waveform 1 S1 at 7 V (see Note B) — 1.5 V — 3.5 V / $V_{OL}$ + 0.3 V $V_{OL}$

$t_{PZH}$ — $t_{PHZ}$ — Output Waveform 2 S1 at Open (see Note B) — 1.5 V — $V_{OH}$ − 0.3 V $V_{OH}$ / ≈ 0 V

NOTES:  A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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