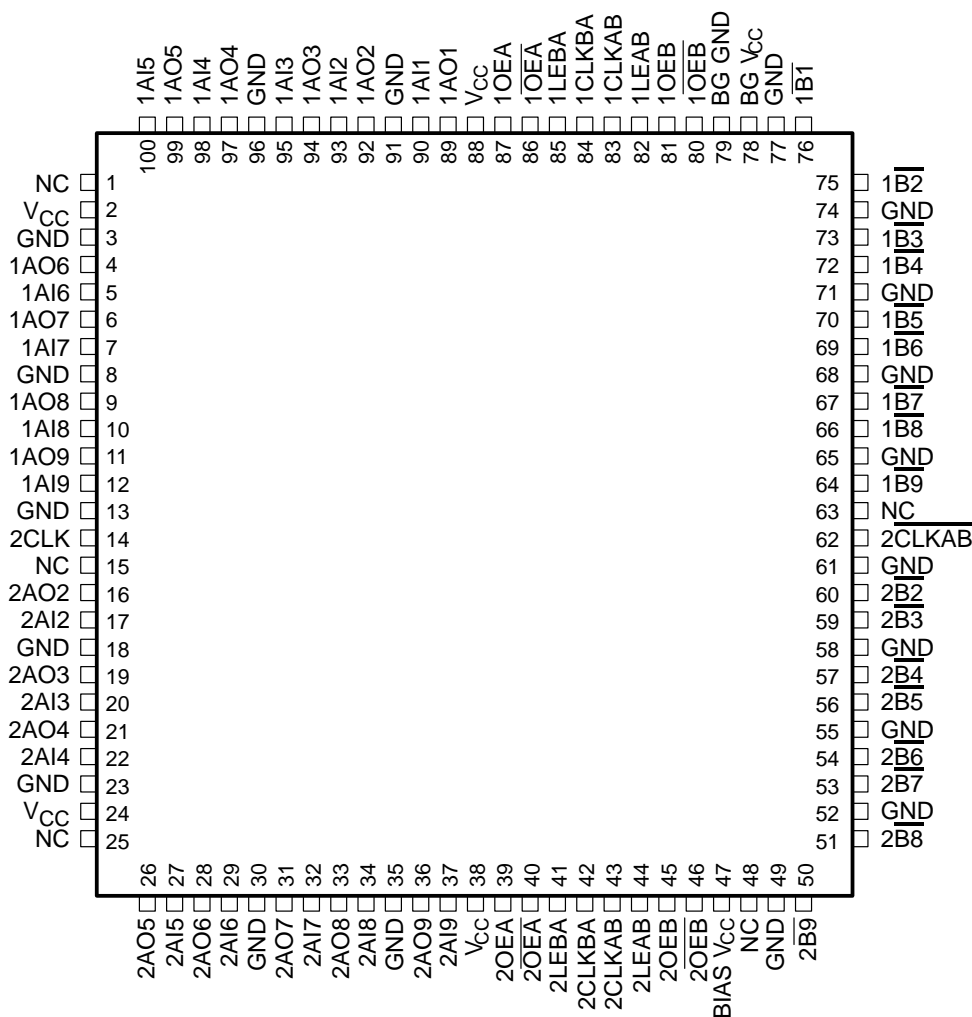


SN54FB1651, SN74FB1651 17-BIT TTL/BTL UNIVERSAL STORAGE TRANSCEIVERS WITH BUFFERED CLOCK LINES

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- Compatible With IEEE Std 1194.1-1991 (BTL)
- TTL A Port, Backplane Transceiver Logic (BTL) \bar{B} Port
- Open-Collector \bar{B} -Port Outputs Sink 100 mA
- BIAS V_{CC} Minimizes Signal Distortion During Live Insertion or Withdrawal
- High-Impedance State During Power Up and Power Down
- \bar{B} -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping to Aid in Line Termination
- Package Options Include High-Power Shrink Quad Flat (PCA) Package With 0.5-mm Pin Pitch and Ceramic Quad Flat (HQA) Package

SN54FB1651 . . . HQA PACKAGE
SN74FB1651 . . . PCA PACKAGE
(TOP VIEW)



NC – No internal connection



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
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SN54FB1651, SN74FB1651

17-BIT TTL/BTL UNIVERSAL STORAGE TRANSCEIVERS

WITH BUFFERED CLOCK LINES

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description

The 'FB1651 contain an 8-bit and a 9-bit transceiver with a buffered clock. The clock and the transceivers are designed to translate signals between TTL and backplane transceiver logic (BTL) environments. They are specifically designed to be compatible with IEEE Std 1194.1-1991.

The \bar{B} port operates at BTL-signal levels. The open-collector \bar{B} ports are specified to sink 100 mA. Two output enables (OEB and \overline{OEB}) are provided for the \bar{B} outputs. When OEB is low, \overline{OEB} is high, or V_{CC} is less than 2.1 V, the \bar{B} port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the \bar{B} port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

The SN54FB1651 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74FB1651 is characterized for operation from 0°C to 70°C .

Function Tables

TRANSCEIVER

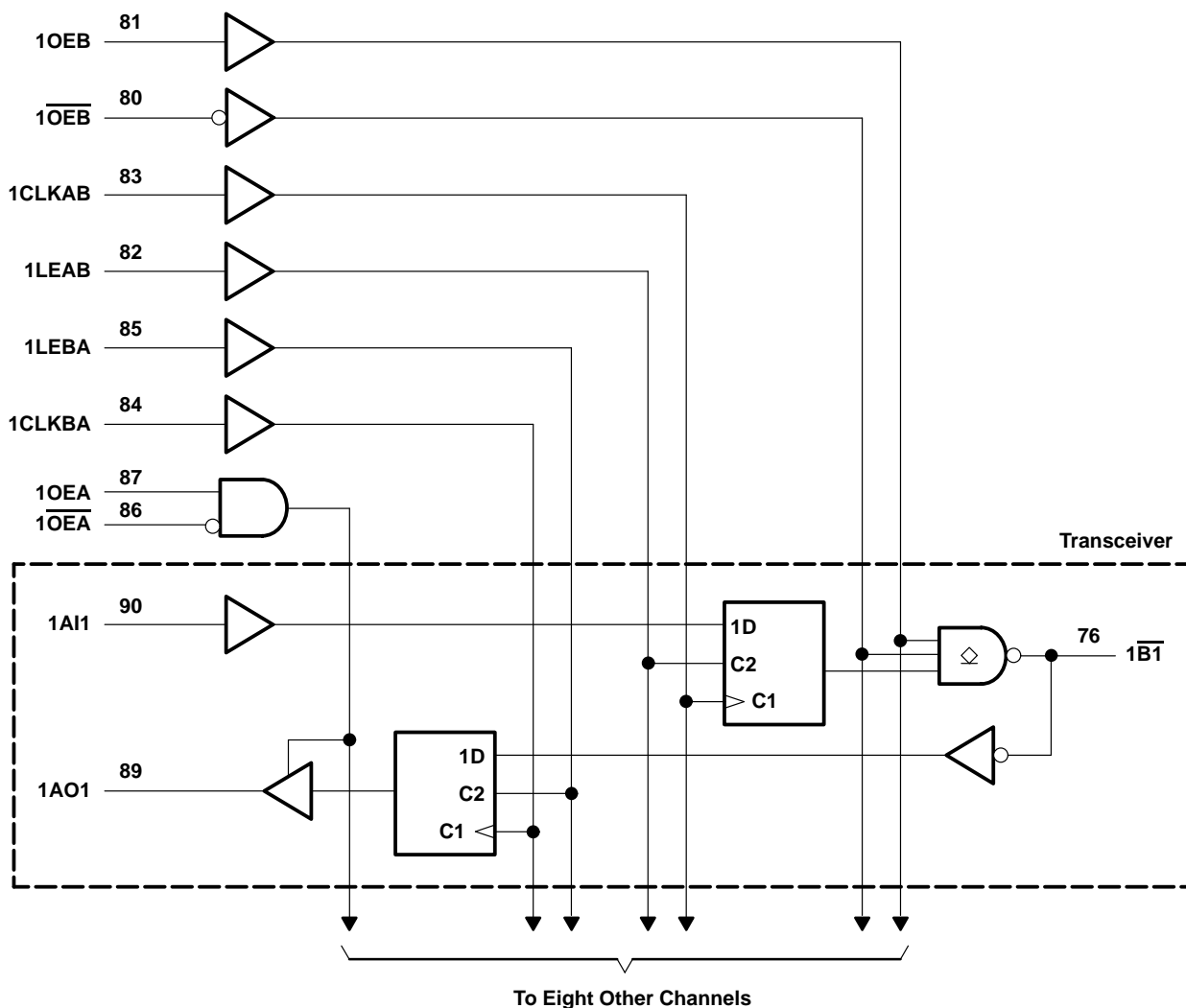
INPUTS				FUNCTION
\overline{OEA}	OEA	OEB	\overline{OEB}	
X	X	H	L	\bar{A} data to B bus
L	H	X	X	\bar{B} data to A bus
L	H	H	L	\bar{A} data to B bus, \bar{B} data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

STORAGE MODE

INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	\uparrow	Store data
L	L	Storage

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functional block diagram



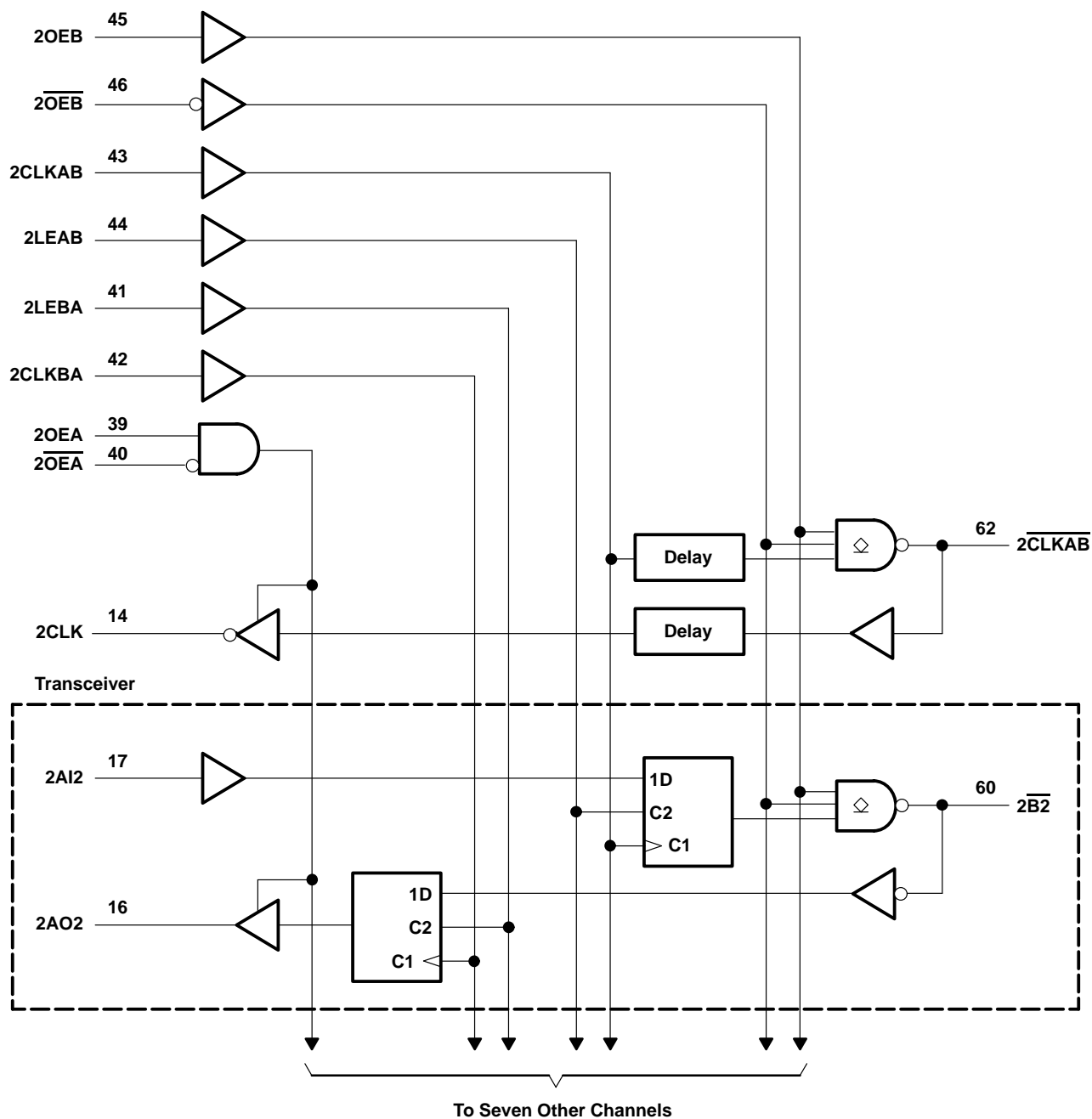
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functional block diagram (continued)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} , BIAS V_{CC} , BG V_{CC}	–0.5 V to 7 V
Input voltage range, V_I : Except \bar{B} port	–1.2 V to 7 V
\bar{B} port	–1.2 V to 3.5 V
Voltage range applied to any \bar{B} output in the disabled or power-off state, V_O	–0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O	–0.5 V to V_{CC}
Input clamp current, I_{IK} : Except \bar{B} port	–40 mA
\bar{B} port	–18 mA
Current applied to any single output in the low state, I_O : A port	48 mA
\bar{B} port	200 mA
Package thermal impedance, θ_{JA} (see Note 1): PCA package	33°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 2)

			SN54FB1651			SN74FB1651			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} , BG V_{CC} , BIAS V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	\bar{B} port	1.62		2.3	1.62		2.3	V
		Except \bar{B} port	2			2			
V_{IL}	Low-level input voltage	\bar{B} port	0.75		1.47	0.75		1.47	V
		Except \bar{B} port			0.8			0.8	
I_{IK}	Input clamp current				–18			–18	mA
I_{OH}	High-level output current	A port			–3			–3	mA
I_{OL}	Low-level output current	A port			24			24	mA
		\bar{B} port			100			100	
T_A	Operating free-air temperature		–55		125	0		70	°C

NOTE 2: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB1651			SN74FB1651			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	B̄ port	V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2			V
	Except B̄ port	V _{CC} = 4.5 V, I _I = −40 mA		−0.5			−0.5			
V _{OH}	AO port	V _{CC} = 4.5 V	I _{OH} = −1 mA							V
			I _{OH} = −3 mA	2.5	3.3	2.5	3.3			
V _{OL}	AO port	V _{CC} = 4.5 V,	I _{OL} = 24 mA	0.35 0.5		0.35 0.5		V		
	B̄ port	V _{CC} = 4.5 V	I _{OL} = 80 mA	0.75 1.1		0.75 1.1				
			I _{OL} = 100 mA	1.15		1.15				
I _I	Except B̄ port	V _{CC} = 5.5 V,	V _I = 5.5 V	50			50			μA
I _{IH} ‡	Except B̄ port	V _{CC} = 5.5 V,	V _I = 2.7 V	50			50			μA
I _{IL} ‡	Except B̄ port	V _{CC} = 5.5 V,	V _I = 0.5 V	−50			−50			μA
	B̄ port	V _{CC} = 5.5 V,	V _I = 0.75 V	−100			−100			
I _{OZH}	AO port	V _{CC} = 5.5 V,	V _O = 2.7 V	50			50			μA
I _{OZL}	AO port	V _{CC} = 5.5 V,	V _O = 0.5 V	−50			−50			μA
I _{OZPU} §	AO port	V _{CC} = 0 to 2.1 V,	V _O = 0.5 V to 2.7 V	50			50			μA
I _{OZPD} §	AO port	V _{CC} = 2.1 V to 0,	V _O = 0.5 V to 2.7 V	−50			−50			μA
I _{OH}	B̄ port	V _{CC} = 0 to 5.5 V,	V _O = 2.1 V	100			100			μA
I _{OS} ¶	A port	V _{CC} = 5.5 V,	V _O = 0	−30	−150		−30	−150		mA
I _{CC}	A port to B̄ port	V _{CC} = 5.5 V,	I _O = 0	100			100			mA
	B̄ port to A port			120			120			
C _i	AI port	V _I = 0.5 V or 2.5 V		5.5		5.5		pF		
	Control inputs			5.5		5.5				
C _O	AO ports	V _O = 0.5 V or 2.5 V		5.5		5.5		pF		
C _{io} §	B̄ port per IEEE Std 1194.1-1991	V _{CC} = 0 to 5.5 V		5.5		5.5		pF		

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ This parameter is warranted but not production tested.

¶ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB1651		SN74FB1651		UNIT	
				MIN	MAX	MIN	MAX		
I _{CC} (BIAS V _{CC})		V _{CC} = 0 to 4.5 V	V _B = 0 to 2 V, V _I (BIAS V _{CC}) = 4.5 V to 5.5 V		450		450		μA
		V _{CC} = 4.5 V to 5.5 V			10		10		
V _O	B̄ port	V _{CC} = 0, V _I (BIAS V _{CC}) = 5 V		1.62	2.1	1.62	2.1	V	
I _O	B̄ port	V _{CC} = 0, V _B = 1 V, V _I (BIAS V _{CC}) = 4.5 V to 5.5 V		-1		-1		μA	
		V _{CC} = 0 to 5.5 V, OEB = 0 to 0.8 V		100		100			
		V _{CC} = 0 to 2.2 V, OEB = 0 to 5 V		100		100			

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WITH BUFFERED CLOCK LINES
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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V _{CC} = 5 V, T _A = 25°C		SN54FB1651		SN74FB1651				UNIT
							T _A = 0°C to 70°C		T _A = −40°C to 85°C		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN†	MAX†	
f _{clock}	Clock frequency		0	150	0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK or LE		3.3		3.3		3.3		3.3		ns
t _{su}	Setup time	Data before LE	4.8		5.5		4.8		5.5		ns
		Data before CLK↑	4.9		5.5		4.6		5.5		
t _h	Hold time	Data after LE	1.8		1.8		1.8		1.8		ns
		Data after CLK↑	1.1		1.1		1.1		1.1		

[†] These parameters are warranted but not production tested.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54FB1651		SN74FB1651				UNIT
								T _A = 0°C to 70°C		T _A = -40°C to 85°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN†	MAX†	
f _{max}			150			150		150		150		MHz
t _{PLH}	AI	\overline{B}	1.8	3.7	5.3	1.8	6.6	1.8	6.2	1.8	6.3	ns
t _{PHL}			2.9	4.4	6	2.9	7.3	2.9	6.6	2.9	7.2	
t _{PLH}	LEAB	\overline{B}	2.7	4.2	5.8	2.7	6.9	2.7	6.4	2.7	6.5	ns
t _{PHL}			3.5	5	6.5	3.5	7.5	3.5	7.3	3.5	7.3	
t _{PLH}	CLKAB	\overline{B}	2.3	3.9	5.5	2.3	6.5	2.3	6	2.3	6.1	ns
t _{PHL}			2.9	4.5	6.1	2.9	6.8	2.9	6.7	2.9	6.7	
t _{PLH}	2CLKAB	$\overline{2CLKAB}$	4.6	6.9	8.8	4.6	10.7	4.6	9.9	4.6	10.2	ns
t _{PHL}			4.9	6.5	8.1	4.9	9.2	4.9	8.8	4.9	8.9	
t _{PLH}	\overline{B}	AO	3.5	5.9	7.9	3.5	9.7	3.5	8	3.5	8.9	ns
t _{PHL}			2.2	3.7	5.3	2.2	6	2.2	5.7	2.2	5.8	
t _{PLH}	LEBA	AO	1.8	3.2	4.6	1.8	5.4	1.8	5.1	1.8	5.2	ns
t _{PHL}			1.7	3	4.4	1.7	5.1	1.7	4.7	1.7	4.8	
t _{PLH}	CLKBA	AO	1.8	3.1	4.6	1.8	5.4	1.8	5.1	1.8	5.1	ns
t _{PHL}			1.7	3.1	4.6	1.7	5.3	1.7	4.9	1.7	5	
t _{PLH}	$\overline{2CLKAB}$	2CLK	6.4	9.7	11.8	6.4	15	6.4	13.4	6.4	13.8	ns
t _{PHL}			4.1	6.9	8.9	4.1	11.2	4.1	10.3	4.1	10.5	
t _{PLH}	OEB	\overline{B}	2.7	4.6	6.4	2.7	7.4	2.7	6.7	2.7	7	ns
t _{PHL}			2.9	4.1	5.9	2.9	6.8	2.9	6.6	2.9	6.6	
t _{PLH}	\overline{OEB}	\overline{B}	2.6	4.3	6.2	2.6	7.2	2.6	6.6	2.6	6.7	ns
t _{PHL}			3.4	4.6	6.4	3.4	7.2	3.4	7	3.4	7	
t _{PZH}	OEA	AO	1.4	2.9	4.4	1.4	5.3	1.4	4.9	1.4	5	ns
t _{PZL}			1.4	2.6	4	1.4	4.9	1.4	4.6	1.4	4.7	
t _{PHZ}	OEA	AO	1.7	3.4	5.1	1.7	5.9	1.7	5.8	1.7	5.8	ns
t _{PLZ}			2.2	3.6	5	2.2	5.8	2.2	5.5	2.2	5.6	
t _{PZH}	\overline{OEA}	AO	1.7	3.3	4.7	1.7	5.9	1.7	5.5	1.7	5.6	ns
t _{PZL}			1.7	3.1	4.4	1.7	5.4	1.7	5.1	1.7	5.2	
t _{PHZ}	\overline{OEA}	AO	1.5	2.9	4.5	1.5	5.2	1.5	5.1	1.5	5.1	ns
t _{PLZ}			2	3.1	4.6	2	5	2	4.8	2	4.8	
t _t	Transition time†	\overline{B} outputs (1.3 V to 1.8 V)	0.9	1.7		0.3	6.8	0.5	4.6	0.5	4.6	ns
		AO outputs (10% to 90%)	0.5	2		0.3	4.3	0.4	4.2	0.4	4.2	
\overline{B} -port input pulse rejection†			1			1		1		1		ns

† These parameters are warranted but not production tested.

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output skew characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			V _{CC} = 5 V, T _A = 25°C			SN54FB1651		SN74FB1651		UNIT
			MIN	TYP	MAX†	MIN	MAX†	MIN	MAX†	
t _{sk(p)} ‡	Skew between drivers switching in any direction in the same package	CLK to \overline{B} and 2CLKAB						4	ns	
		CLK to \overline{B}						1.5		
t _{sk(p)} §	Skew for any single channel t _{PHL} –t _{PLH}	A1 to \overline{B} or \overline{B} to AO		1					ns	
t _{sk(o)} §	Skew between drivers in the same package	A1 to \overline{B} or \overline{B} to AO		0.5					ns	

† These parameters are warranted but not production tested.

‡ Skew values are applicable for CLK mode only.

§ Skew values are applicable for through mode only.

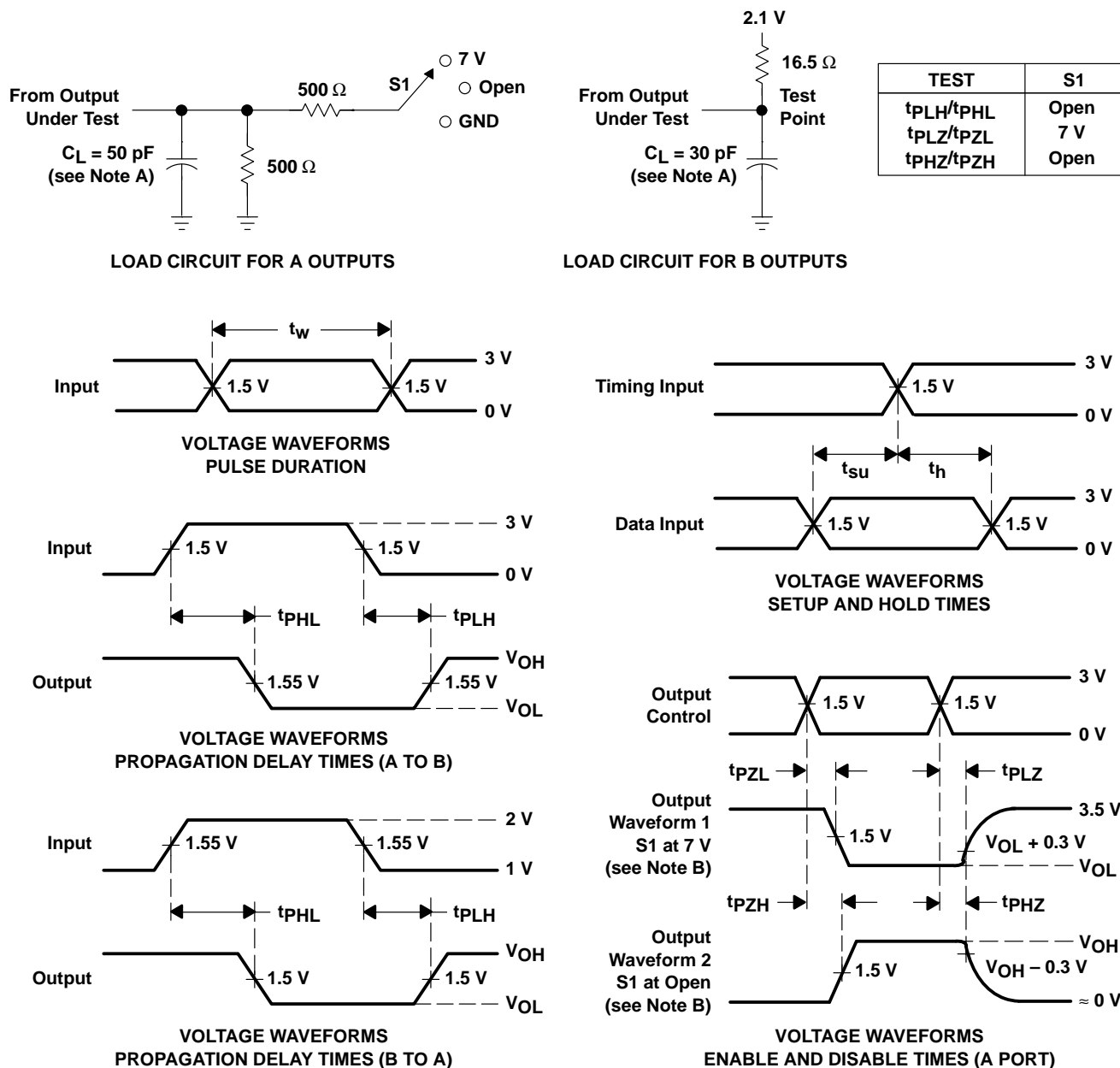
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17-BIT TTL/BTL UNIVERSAL STORAGE TRANSCEIVERS

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: TTL inputs: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns; BTL inputs: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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