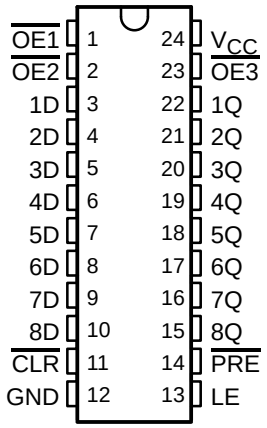
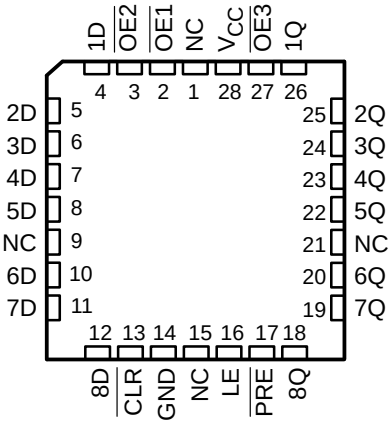
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54ABT845 . . . JT PACKAGE
SN74ABT845 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ABT845 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’ABT845 9-bit latch is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

Since clear ($\overline{CLR}$) and preset ($\overline{PRE}$) are independent of the clock, taking the $\overline{CLR}$ input low causes the eight Q outputs to go low. Taking the $\overline{PRE}$ input low will cause the eight Q outputs to go high. When both $\overline{PRE}$ and $\overline{CLR}$ are taken low, the outputs go high.

The buffered output-enable ($\overline{OE1}$, $\overline{OE2}$, and $\overline{OE3}$) inputs can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable inputs do not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT845 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT845 is characterized for operation from –40°C to 85°C.

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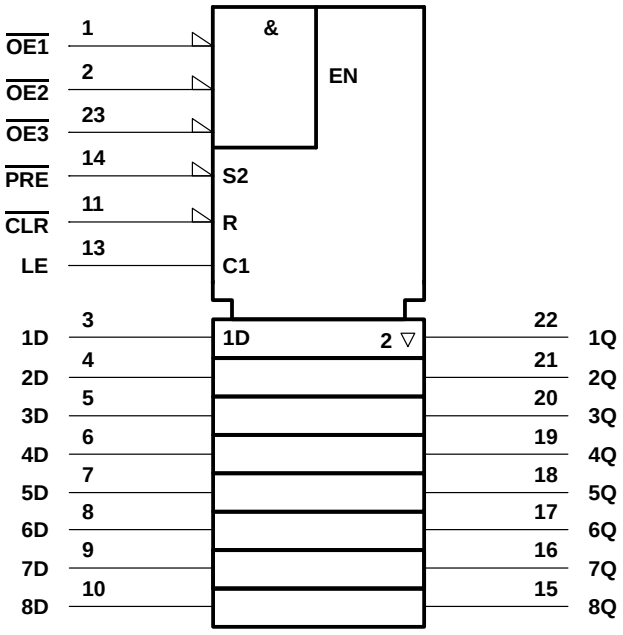
FUNCTION TABLE

INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE1}$	$\overline{OE2}$	$\overline{OE3}$	LE	D	Q
L	X	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

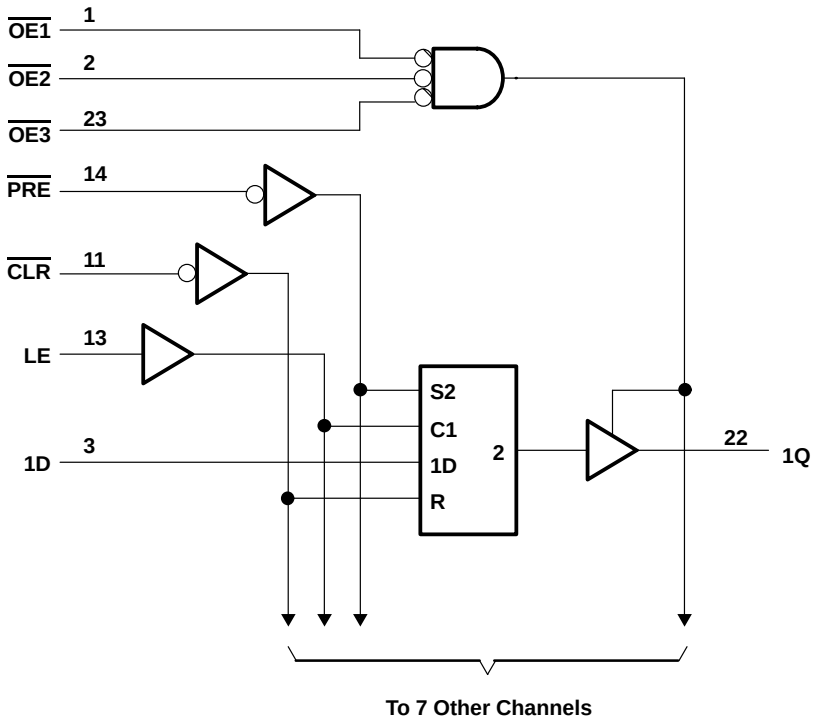
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT845 . . . . . 96 mA
SN74ABT845 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air): DW package . . . . . 1 W
NT package . . . . . 1.3 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

		SN54ABT845		SN74ABT845		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT845		SN74ABT845		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = –3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = –3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = –24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = –32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				–50		–50		–50	µA
I_{OFF}	V_{CC} = 0 V, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		–50	–140	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V									pF
C_o	V_O = 2.5 V or 0.5 V									pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT845		SN74ABT845		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low							ns
		$\overline{PRE}$ low							
		LE high							
t_{su}	Setup time, data before LE↓	High							ns
		Low							
t_h	Hold time, data after LE↓								ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT845		SN74ABT845		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q								ns
t_{PHL}										
t_{PLH}	LE	Q								ns
t_{PHL}										
t_{PLH}	PRE	Q								ns
t_{PHL}										
t_{PLH}	CLR	Q								ns
t_{PHL}										
t_{PZH}	OE	Q								ns
t_{PZL}										
t_{PHZ}	OE	Q								ns
t_{PLZ}										

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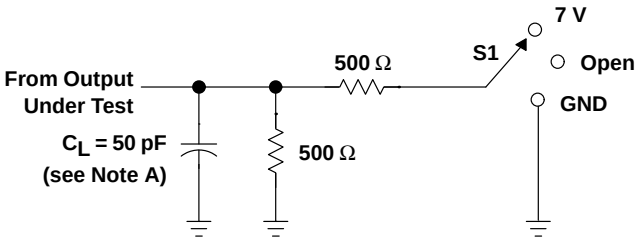
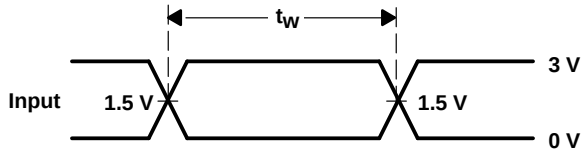
PARAMETER MEASUREMENT INFORMATION

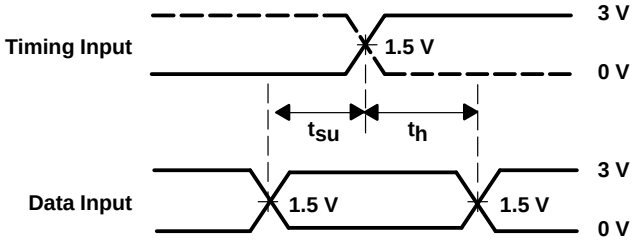


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

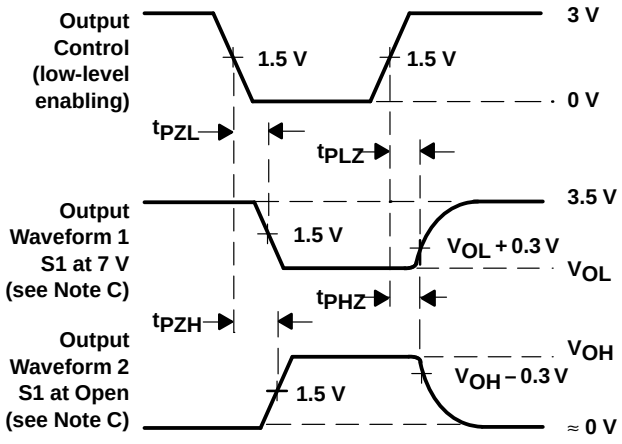
LOAD CIRCUIT FOR OUTPUTS



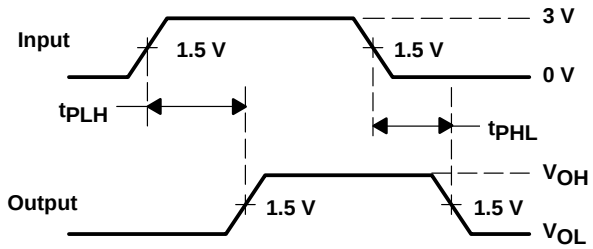
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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