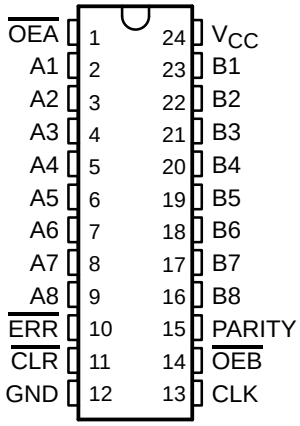
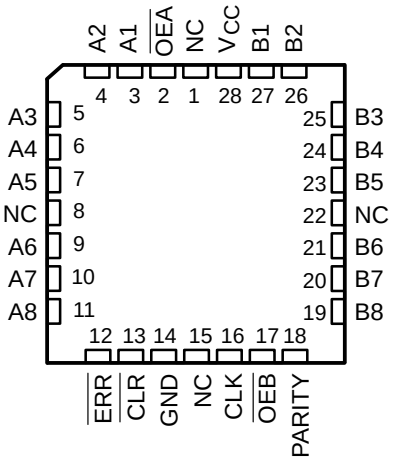
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Parity Error Flag With Parity Generator/Checker**
- **Register for Storage of the Parity Error Flag**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54ABT834 . . . JT PACKAGE
SN74ABT834 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ABT834 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’ABT834 8-bit to 9-bit parity transceiver is designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error ($\overline{ERR}$) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{OEA}$ and $\overline{OEB}$) inputs can be used to disable the device so that the buses are effectively isolated. The ’ABT834 provides inverted data at its outputs.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the $\overline{ERR}$ flag. The parity-error output is clocked into the register on the rising edge of the clock (CLK) input. The error flag register is cleared with a low pulse on the clear ($\overline{CLR}$) input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT834 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT834 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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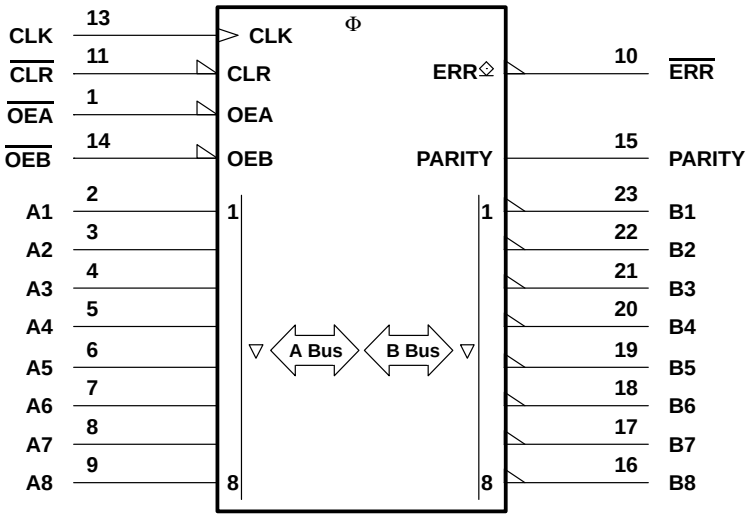
FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
OEB	OEA	CLR	CLK	Ai Σ OF H's	Bi† Σ OF L's	A	B	PARITY	ERR‡	
L	H	X	X	Odd Even	NA	NA	$\overline{A}$	H L	NA	$\overline{A}$ data to B bus and generate parity
H	L	H	↑	NA	Odd Even	$\overline{B}$	NA	NA	H L	$\overline{B}$ data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error flag register
H	H	H L H H	No↑ No↑ ↑ ↑	X X O Even	d X d	Z	Z	Z	NC H L H	Isolation§
L	L	X	X	Odd Even	NA	NA	$\overline{A}$	L H	NA	$\overline{A}$ data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume the $\overline{ERR}$ output was previously high.
§ In this mode, the $\overline{ERR}$ output (when clocked) shows inverted parity of the A bus.

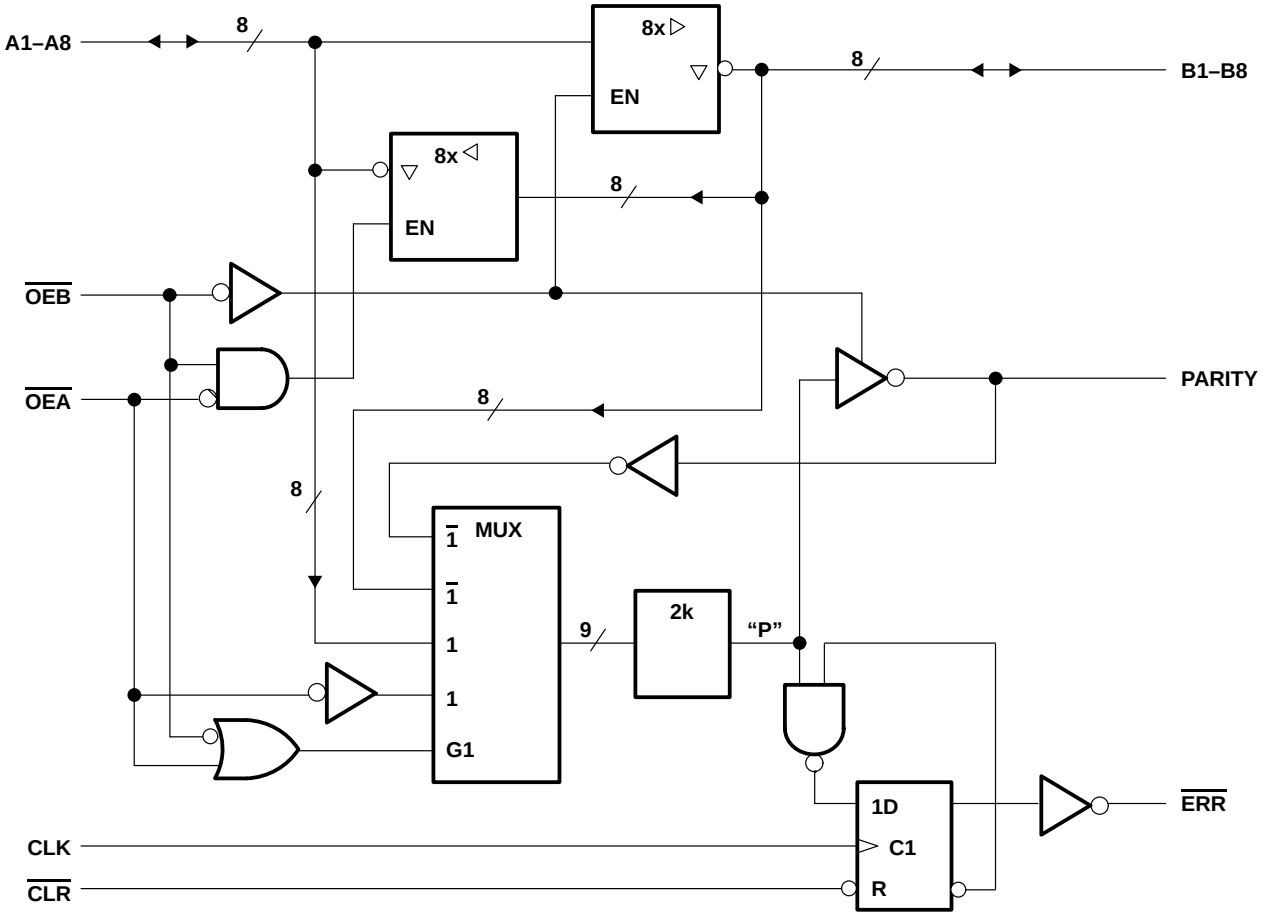
PRODUCT PREVIEW

logic symbol¶



¶ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



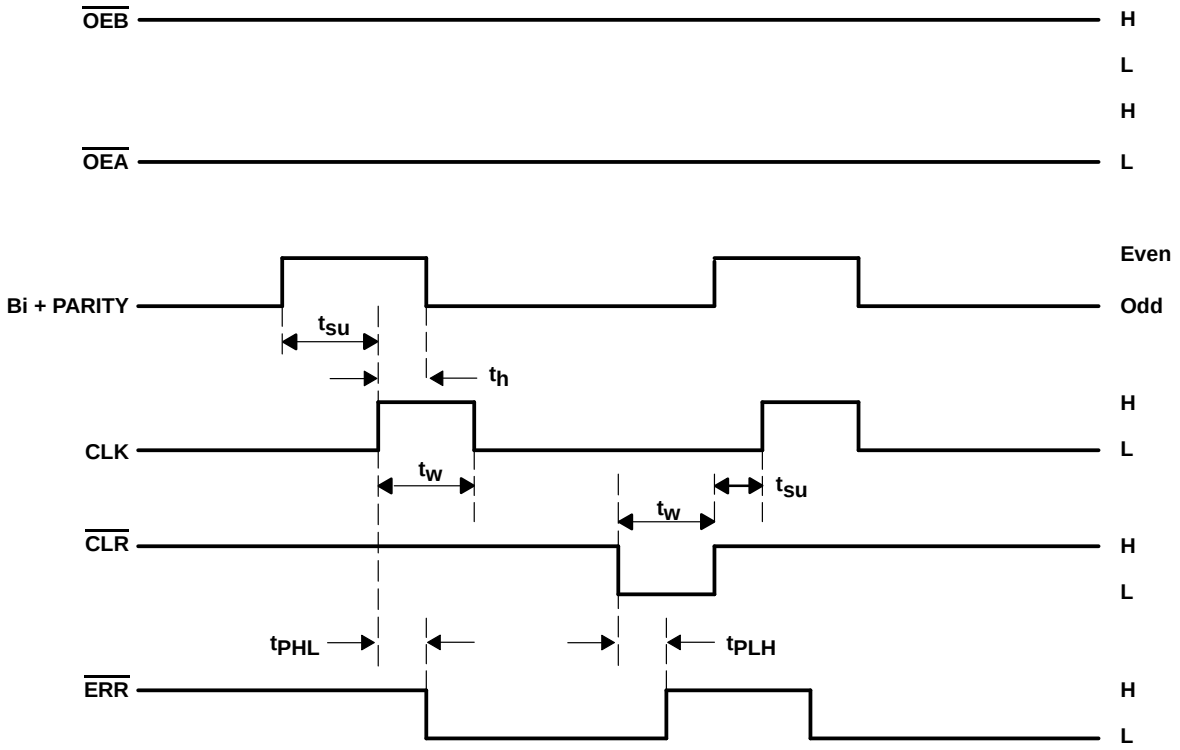
ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT $\overline{ERR}$	FUNCTION
$\overline{CLR}$	CLK	POINT "P"	$\overline{ERR}_{n-1}$†		
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

† The state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, CLK, or point "P".

PRODUCT PREVIEW

error-flag waveforms



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT834 . . . . . 96 mA
SN74ABT834 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air): DW package . . . . . 1 W
NT package . . . . . 1.3 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			SN54ABT834		SN74ABT834		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{OH}	High-level output voltage	$\overline{ERR}$		5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current	Except $\overline{ERR}$		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT834		SN74ABT834		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA	All outputs except $\overline{ERR}$	2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = –24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = –32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 24 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 4.5 V	$\overline{ERR}$								µA
I_I	V_{CC} = 5.5 V,		Control inputs			±1		±1		±1	µA
	V_I = V_{CC} or GND		A or B ports			±100		±100		±100	
I_{IL}	V_{CC} = 0 V,	V_I = GND	A or B ports			–50		–50		–50	µA
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{OFF}	V_{CC} = 0 V,	V_I or $V_O \le$ 5.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V,	A or B ports	Outputs high		1	250		250		250	µA
	I_O = 0,		Outputs low		24	30		30		30	mA
	V_I = V_{CC} or GND		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V,	One input at 3.4 V, Other inputs at V_{CC} or GND				50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V		Control inputs								pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports								pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT834		SN74ABT834		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high							ns
		CLK low							
		$\overline{CLR}$ low							
t_{su}	Setup time before CLK↑	A port							ns
		$\overline{CLR}$							
t_h	Hold time after CLK↑	A port							ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

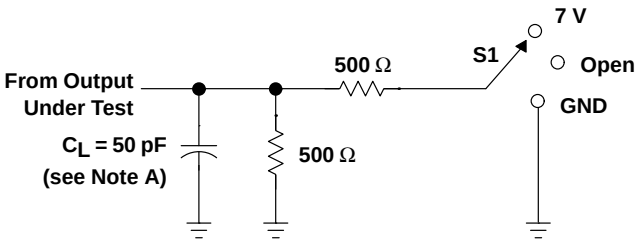
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT834		SN74ABT834		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PZH}	OE	A or B								ns
t_{PZL}										
t_{PHZ}	OE	A or B								ns
t_{PLZ}										
t_{PLH}	A or OE	PARITY								ns
t_{PHL}										
t_{PLH}	$\overline{CLR}$	ERR								ns
t_{PHL}	CLK									

PRODUCT PREVIEW

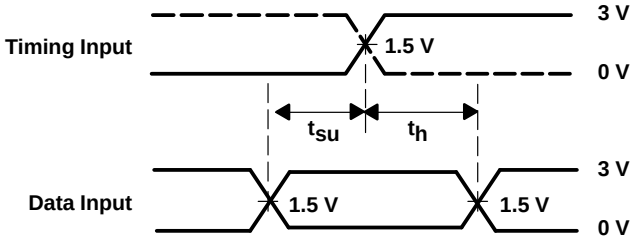
PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

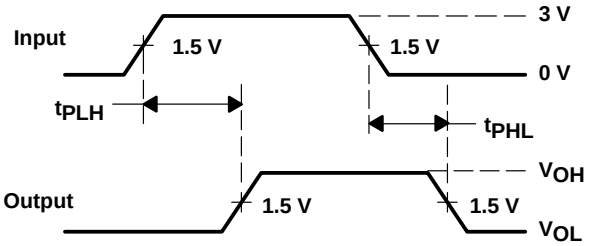
$\overline{ERR}$	S1
t_{PHL} (see Note E)	Open
t_{PLH} (see Note F)	7 V



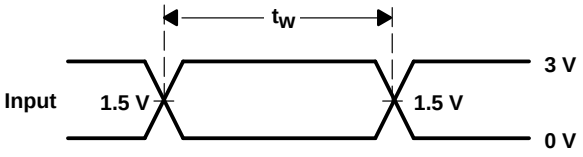
LOAD CIRCUIT FOR OUTPUTS



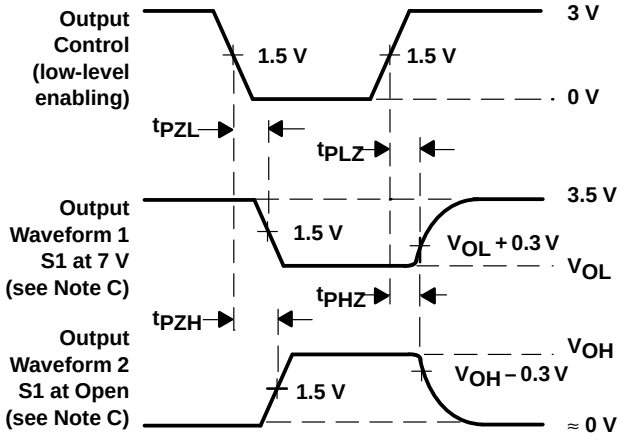
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PHL} is measured at 1.5 V.
F. t_{PLH} is measured at V_{OL} + 0.3 V.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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