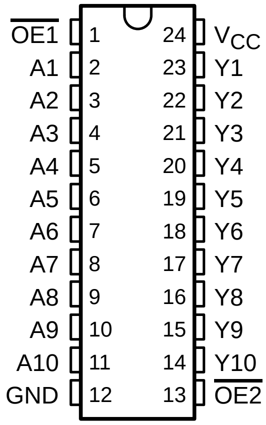
SN54ABT827, SN74ABT827
10-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

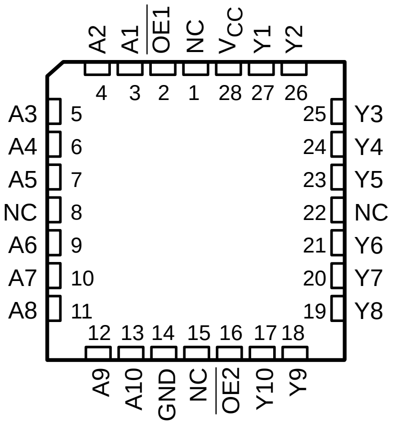
SCBS159D – JANUARY 1991 – REVISED MAY 1997

- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs**

SN54ABT827 . . . JT PACKAGE
SN74ABT827 . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT827 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 10-bit buffers or bus drivers provide a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state. The ’ABT827 provide true data at the outputs.

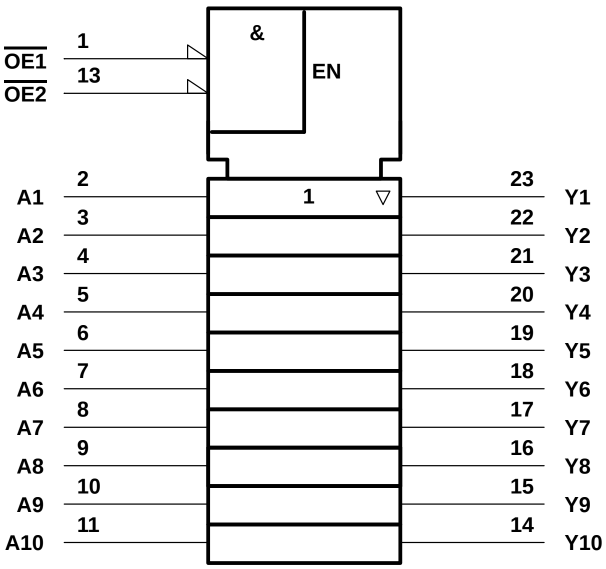
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT827 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT827 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

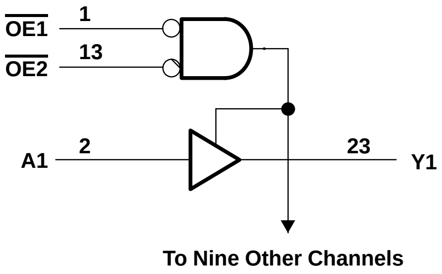
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}		–0.5 V to 7 V
Input voltage range, V_I (see Note 1)		–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O		–0.5 V to 5.5 V
Current into any output in the low state, I_O:	SN54ABT827	96 mA
	SN74ABT827	128 mA
Input clamp current, I_{IK} ($V_I < 0$)		–18 mA
Output clamp current, I_{OK} ($V_O < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	104°C/W
	DW package	81°C/W
	NT package	67°C/W
	PW package	120°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ABT827		SN74ABT827		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		µs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT827		SN74ABT827		UNIT
			MIN	TYP[†]	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA	3			3		3		
	V_{CC} = 4.5 V	I_{OH} = –24 mA	2			2				
		I_{OH} = –32 mA	2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
		I_{OL} = 64 mA			0.55*				0.55	
V_{hys}				100						mV
I_I	V_{CC} = 0 to 5.5 V,	$V_I = V_{CC}$ or GND			±1		±1		±1	µA
I_{OZPU}[‡]	V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±10		±50	µA
I_{OZPD}[‡]	V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±10		±50	µA
I_{OZH}	V_{CC} = 2.1 V to 5.5 V, V_O = 2.7 V, $\overline{OE} \geq 2$ V				10[§]		10		10[§]	µA
I_{OZL}	V_{CC} = 2.1 V to 5.5 V, V_O = 0.5 V, $\overline{OE} \geq 2$ V				–10[§]		–10		–10[§]	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \leq 4.5$ V			±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O[¶]	V_{CC} = 5.5 V,	V_O = 2.5 V	–50	–140	–225[§]	–50	–225[§]	–50	–225[§]	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, $V_I = V_{CC}$ or GND	Outputs high		80	250		250		250	µA
		Outputs low		35	40[§]		40[§]		40[§]	mA
		Outputs disabled		80	250		250		250	µA
ΔI_{CC}[#]	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			50		50		50	µA
		Control inputs			1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			4						pF
C_o	V_O = 2.5 V or 0.5 V			8						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

[†] All typical values are at V_{CC} = 5 V.

[‡] This parameter is characterized, but not production tested.

[§] This data sheet limit may vary among suppliers.

[¶] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

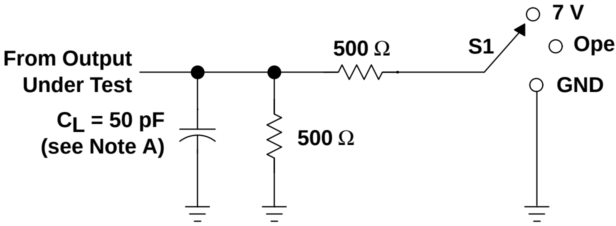
[#] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT827		SN74ABT827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.1	2.6	4.4	1.1	4.9	1.1	4.8	ns
t_{PHL}			1.1	2.3	4.1	1.1	4.8	1.1	4.7	
t_{PZH}	$\overline{OE}$	Y	1[§]	3.2	5.1	1	6	1[§]	5.9	ns
t_{PZL}			1[§]	3.3	5.9	1	7.1	1[§]	6.9	
t_{PHZ}	$\overline{OE}$	Y	2	4.9	6.3	2	7	2	6.8	ns
t_{PLZ}			1.3[§]	4.2	6.6	1.3	7.9	1.3[§]	6.9	

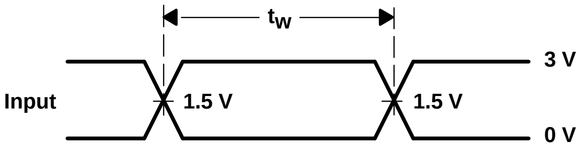
[§] This data sheet limit may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

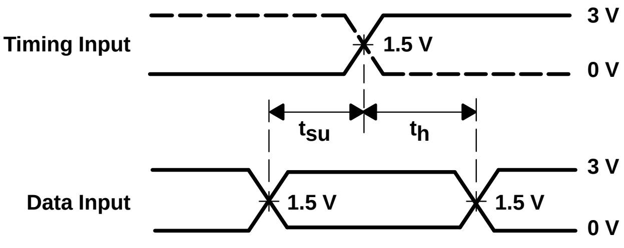


LOAD CIRCUIT

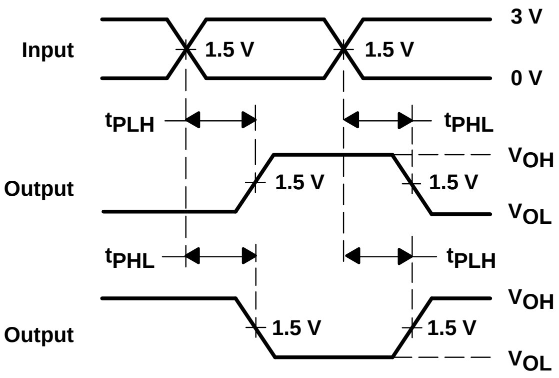
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



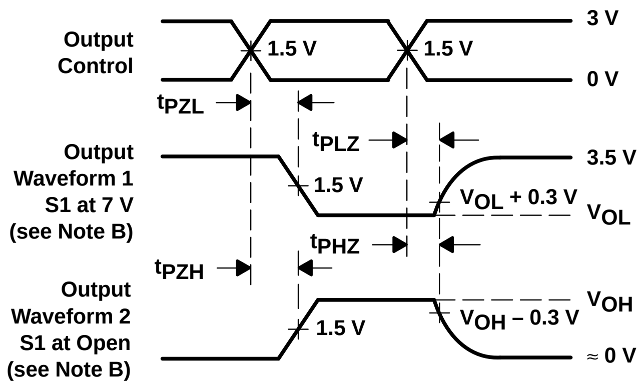
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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